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FINAL REPORT

SPACECRAFT ATOMIC TIME SYSTEM

NASA Contract NAS 9-5425, Part II

Prepared by: GENERAL RADIO COMPANY

NASA CR 102193

RUBIDIUM SPACECRAFT ATOMIC TIMING SYSTEM

Final Report

NASA Contract NAS 9-5425, Part II
(Varian Associates Subcontract VQE-1301)

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For Transmittal to: NASA Manned Spacecraft Center
Houston, Texas

December 12, 1969

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1.1 BACKGROUND INFORMATION

This is the Final Report on Part II of Contract NAS9-5425, between the NASA Manned Spacecraft Center, Houston, Texas and Varian Associates of Palo Alto, California, for the development of a Rubidium Atomic Time and Frequency Reference System for later manned spacecraft use.

Part II of the contract was subcontracted with NASA approval to the General Radio Company, West Concord, Massachusetts, under Varian Subcontract VQE-1301.

The Work Statement applicable to the Part II development of the Spacecraft Atomic Timing System is 67-EE-12, dated November 21, 1967, and as later modified in Amendments 3, 4, and 6 to NAS9-5425.

Details of the deliverable items of hardware and software are given in more detail below.

1.2 HARDWARE REQUIREMENTS

The contract calls for the delivery of two Engineering Models designed and fabricated to demonstrate the technical soundness of the design of a Spacecraft Atomic Timing System, using a Rubidium reference cell in the frequency stabilizing loop.

Mating connectors for external connection to the "SATS" are required.

1.3 SOFTWARE REQUIREMENTS

1.3.1 REPORTS

Monthly Progress Reports were required and were submitted through Varian to NASA-MSC throughout the performance of the contract. These reports included descriptions of overall progress, indications of current problems and proposed solutions, and discussions of work to be performed in the next monthly reporting period.

A Final Report to document and summarize the results of the entire Part II phase of the Contract was also a requirement. This Final Report is submitted in response to this requirement.

1.3.2 SCHEMATICS AND MECHANICAL DRAWINGS

Three sets of detailed electrical schematics and mechanical drawings are required and are being submitted as a deliverable item. These drawings include detailed parts lists. Certain portions of the Optical Package, Master Oscillator and the sub-contracted Microwave Multiplier-Mixer and Power Supply contain data proprietary to the manufacturers, and are so marked.

An 8 x 10 in film positive reduction of each supplied drawing was prepared and is being submitted as a deliverable item.

1.3.3 INSTRUCTION MANUALS

An Instruction Manual, sufficient to connect to, set up, and operate the "SATS" was prepared and supplied to NASA-MSC.

1.3.4 DESIGN REVIEWS

A Design Review with General Radio, Varian and NASA personnel was held when the design of the Engineering Models was essentially complete, and prior to their construction.

NASA and Varian personnel visited the General Radio facility during the contract for progress review.

A final Design Review is planned for NASA-MSC.

1.4 QUANTUM MECHANICAL PRINCIPLES OF RUBIDIUM FREQUENCY STANDARDS

Their high Q and long-term stability make atomic hyperfine transitions useful for frequency control. The following description of the principles involved, while much simplified, may serve to acquaint the reader with the quantum mechanics involved.

Rubidium, one of the alkali metals, has one single electron in the 5th shell. There are two natural isotopes of rubidium, Rb^{85}, which is stable, and Rb^{87}, which is radioactive with a half-life of 6×10^{10} years (β radiator).

Figure 1 is a simplified energy level diagram for Rb^{87}. The 5S1/2 is the ground state of the 5th shell electron; 5P1/2 and 5P3/2 are the excited states. The quantum numbers, F, designate the hyperfine levels and are determined by the vector sums of the nuclear angular momentum and the electron spin. In the presence of a magnetic field, H, each hyperfine level has a number of Zeeman sublevels designated M_F. M_F is determined by the component of F along the direction of the field H. The $M_F = 0$ sublevel is least dependent on the field H, as the nuclear field is perpendicular to the external field.

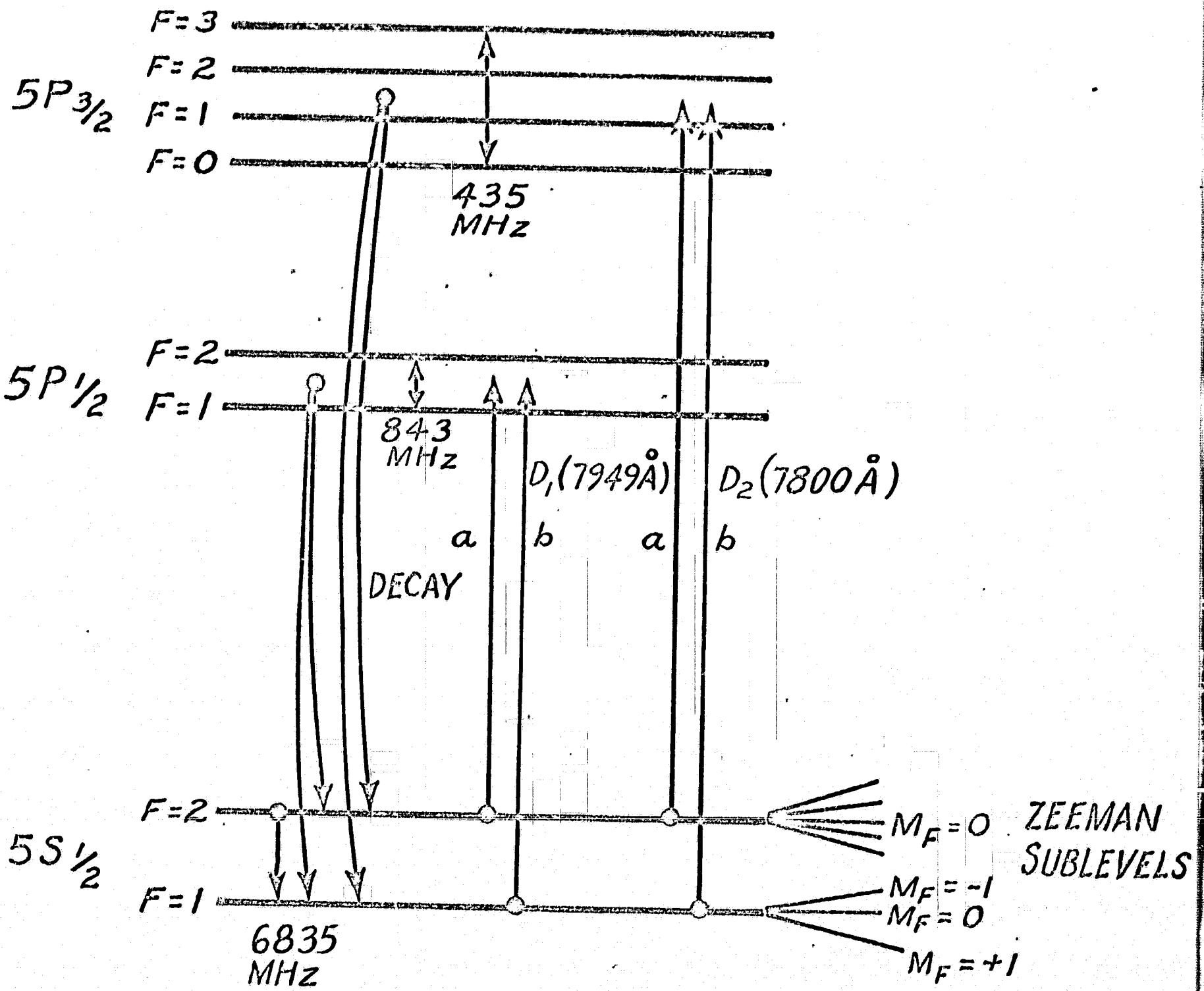
The energy difference between the 5S1/2, $F = 2$, $M_F = 0$, and the 5S1/2, $F = 1$, $M_F = 0$ hyperfine levels corresponds to about 6835 MHz. In order to obtain this transition, an overpopulation in the 5S1/2, $F = 2$ state is required. This population difference can be induced by "optical pumping". Rb^{87} vapor is exposed to light of proper wavelength and the absorption of photon energy pumps some of the atoms from the ground state to the excited states. The atoms remain in the excited states for less than 30 ns and then decay back to the ground state. The energy difference is reradiated. Figure 2 shows the basic transitions involved in the optical pumping process. To produce a population difference between the

F = 2 and F = 1 ground states, it is necessary to pump, selectively, from the F = 1 ground state to one of the excited states. As the probabilities for decay back into the F = 2 and F = 1 ground state are almost equal, the result is a depletion of the F = 1 ground state with respect to the F = 2 ground state, i.e., more atoms in each sublevel of F = 2 than in F = 1.

Figure 1 shows how the various components of the light from a Rb^{87} discharge lamp connect the levels. The light from this lamp contains two major spectral lines, the Rb^{87} D1 line at about 7949 Å, and the Rb^{87} D2 line at about 7800 Å. Absorption of one photon of the D1 line moves one atom from the ground state 5S1/2 to the excited state 5P1/2. Absorption of one photon of the D2 line moves one atom from 5S1/2 to the 5P3/2 state. Each of the D lines consists of two hyperfine components, "a" and "b". The "a" component pumps from the 5S1/2 F = 2 level, and the "b" component from the 5S1/2 F = 1 level.

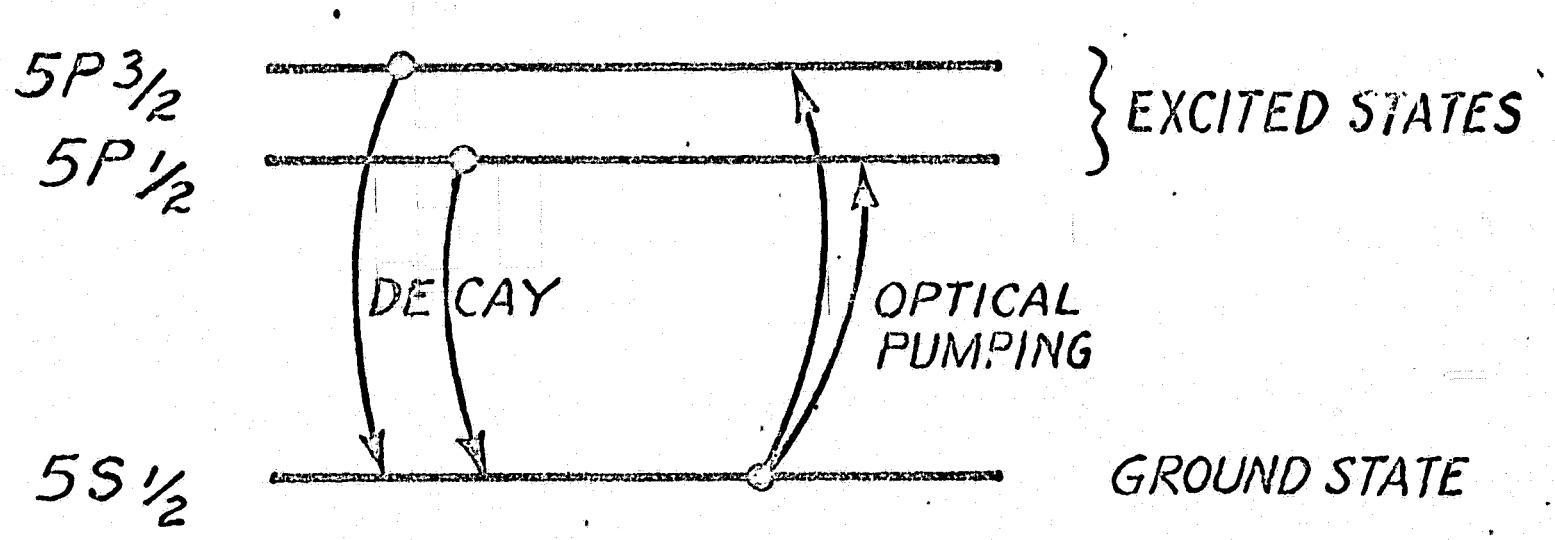
To obtain the desired net population in the 5S1/2, F = 2 state the "a" components of the D lines must be removed. The extremely small difference in wavelength ($\approx$ .06 Å) makes the filter requirements quite stringent. Fortunately, another isotope of rubidium (Rb^{85}) provides the means. The spectral characteristics of the Rb^{85} isotope are quite similar to Rb^{87}, but there is a slight difference in the hyperfine structure. Figure 3 shows the hyperfine spectrum of the Rb^{87} D lines and the Rb^{85} D lines. The "a" component of Rb^{87} D and the "A" component of Rb^{85} D overlap, but there is a difference in wavelength for the Rb^{87} D b and Rb^{85} D B components. As a result, when light from an Rb^{87} lamp is passed through Rb^{85} vapor, the "a" component is absorbed but the "b" component passes the filter cell and pumps from the 5S1/2 F = 1 level in the absorption cell as required.

If a magnetic bias (C field) and a microwave field of proper frequency are applied to the Rb^{87} vapor in the absorption cell, transitions from the over-populated 5S1/2 F = 2 state to the depleted 5S1/2 F = 1 state are stimulated. Each atom reaching the 5S1/2 F = 1 state can then absorb one photon of the pumping light. The absorption of pumping light is detected, and minimum light passed (maximum absorption) indicates proper frequency. The energy gain realized in this type of detection is about 5×10^4, as each radio-photon at 6835 MHz (λ = 4 cm) causes one photon at the D1 line ($\lambda = 8 \times 10^{-5}$ cm) to be absorbed. The light variations are used to adjust the frequency of the RF source. The energy of the 6835 MHz transition is the difference between the energies of the Rb^{87} D1 b component and the decay energy from the 5P1/2 excited state to the 5S1/2 F = 2 ground state, or nearly the same as the difference between the energies of the two hyperfine components of the D1 line. The decay energy (5P1/2 - 5S1/2) is absorbed by collision with buffer gas atoms to prevent optical reradiation. This process is called "quenching".



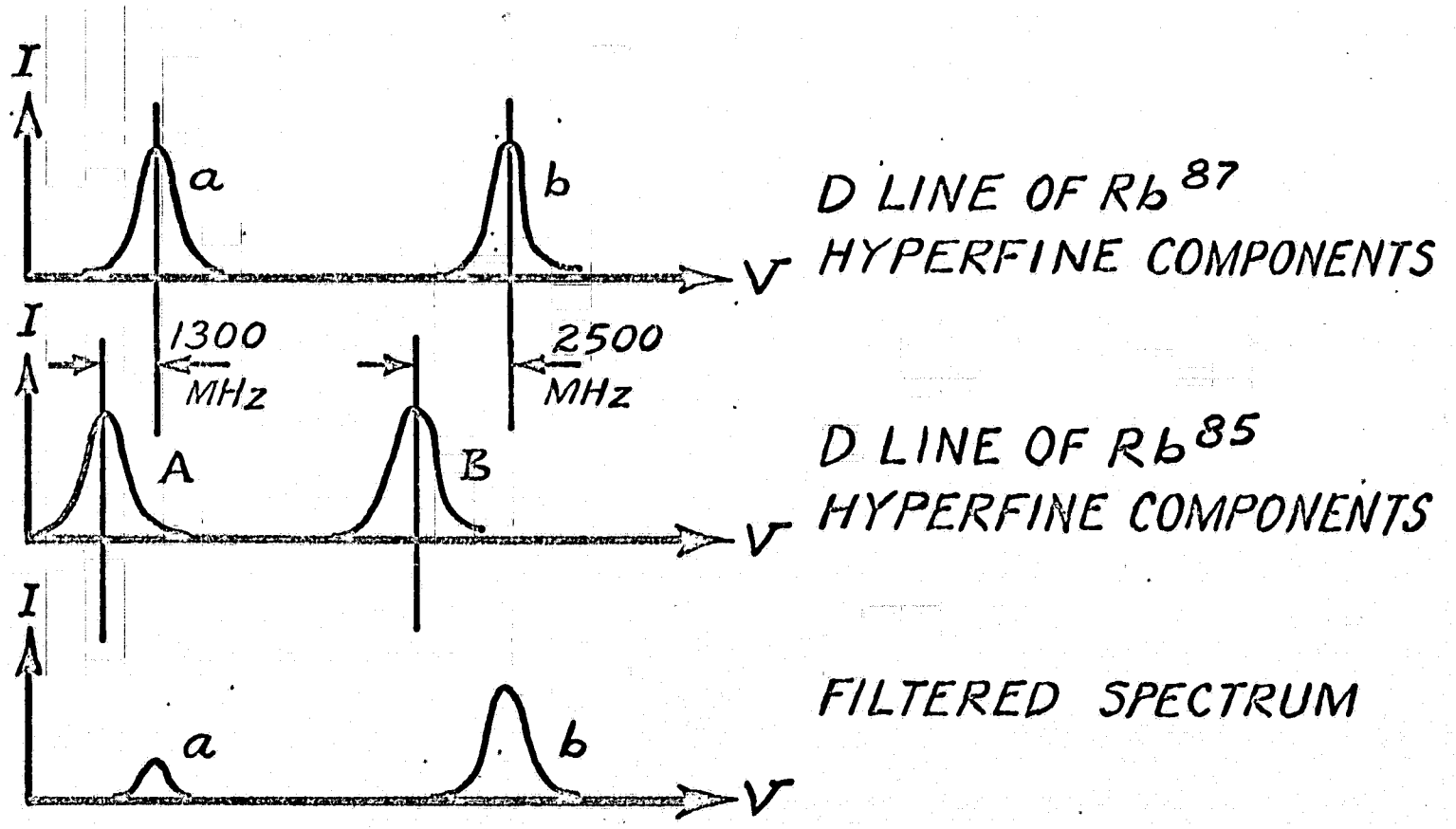
ENERGY LEVELS OF Rb^{87}

fig. 1



OPTICAL PUMPING OF Rb^{87}

fig. 2



ISOTOPE FILTERING OF Rb 87 D LINES

fig. 3

1.5 UTILIZATION OF THE ATOMIC TRANSITION FOR FREQUENCY CONTROL

The quantum mechanical principles discussed in the preceding section are utilized in the SATS rubidium frequency standard to provide a discriminator characteristic which serves as a means to lock the frequency of a Master Crystal Oscillator to the highly stable atomic resonance.

The optical absorption of the Rb^{87} absorption cell inside the Optical Package is maximum when the RF excitation frequency is exactly equal to that of the rubidium resonance. Thus, the photodetector output is a minimum at this excitation frequency; this absorption characteristic is shown in Figure 4 A. A typical rubidium absorption characteristic has a maximum absorption of 0.1% of the total light and a width of a few hundred hertz. This corresponds to a resonance with a Q of 10-20 million.

A triangular waveform at the fundamental modulation frequency is produced by the servo-amplifier "modulation integrator" and applied to an RF phase modulator. This results in square-wave frequency modulation, a signal whose frequency is constant at one value for one half-cycle of the modulation and at another value for the second half-cycle.

When such a signal is used to excite the rubidium discriminator three different situations are possible; the center frequency may be either (1) below, (2) equal to, or (3) above the rubidium resonant frequency.

If the excitation frequency is sufficiently below or above the rubidium "line" no signal at all will be produced. (This would very likely be the case when a unit is first turned on since the Master Crystal Oscillator frequency has a range of several parts per million while the line width is about a thousand times less. Under these conditions the lock detector must sense lack of signal and sweep the frequency toward the line.)

When the center frequency is within the line an error signal is produced. If the excitation center frequency is <u>below</u> the center of the line the photodetector

output will decrease most during the half-cycles of modulation when the frequency is at its higher value. If the excitation center frequency is above the line the output will decrease most during the half-cycles when the frequency is lower. The error signal therefore has a component at the modulation frequency whose phase is 180° different depending on whether the center frequency is below or above the center of the line. This is the rubidium discriminator action used by the frequency lock loop and shown in Figure 4 B. The fundamental signal is a maximum when the center frequency is at the maximum slope of the absorption characteristic and is zero at the center of the line.

At or near the center of the line the excitation frequency passes through the minimum of the absorption characteristic twice per modulation cycle. This results in an error signal component at a frequency equal to twice the modulation rate. This second harmonic signal, while not used by (and indeed a problem for) the frequency lock loop, is used by the lock detector to indicate a locked condition.

Many parameters influence the properties of the rubidium system error signal, most of which are strongly interacting.

Inside the Optical Package these include lamp, filter, and absorption cell construction and operating conditions and also the photodetector efficiency.

Outside the Optical Package, the significant parameters include RF excitation level, modulation rate and modulation deviation.

The resulting signal properties which are significant to the servo-amplifier design and operation are the amplitude and phase (with respect to the modulation signal) of the fundamental and second harmonic signals.

FIG 4A

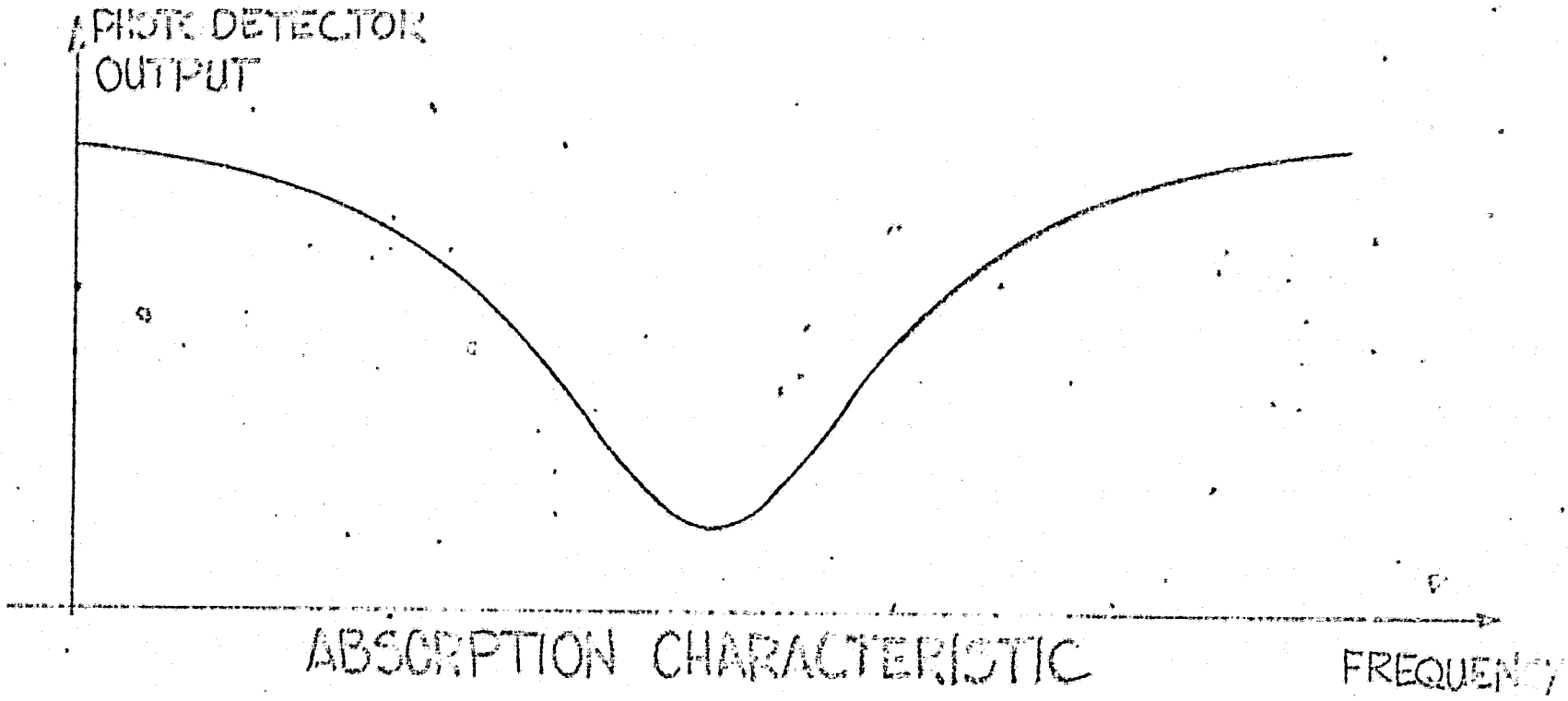


PHOTO DETECTOR
OUTPUT
ABSORPTION CHARACTERISTIC
FREQUENCY

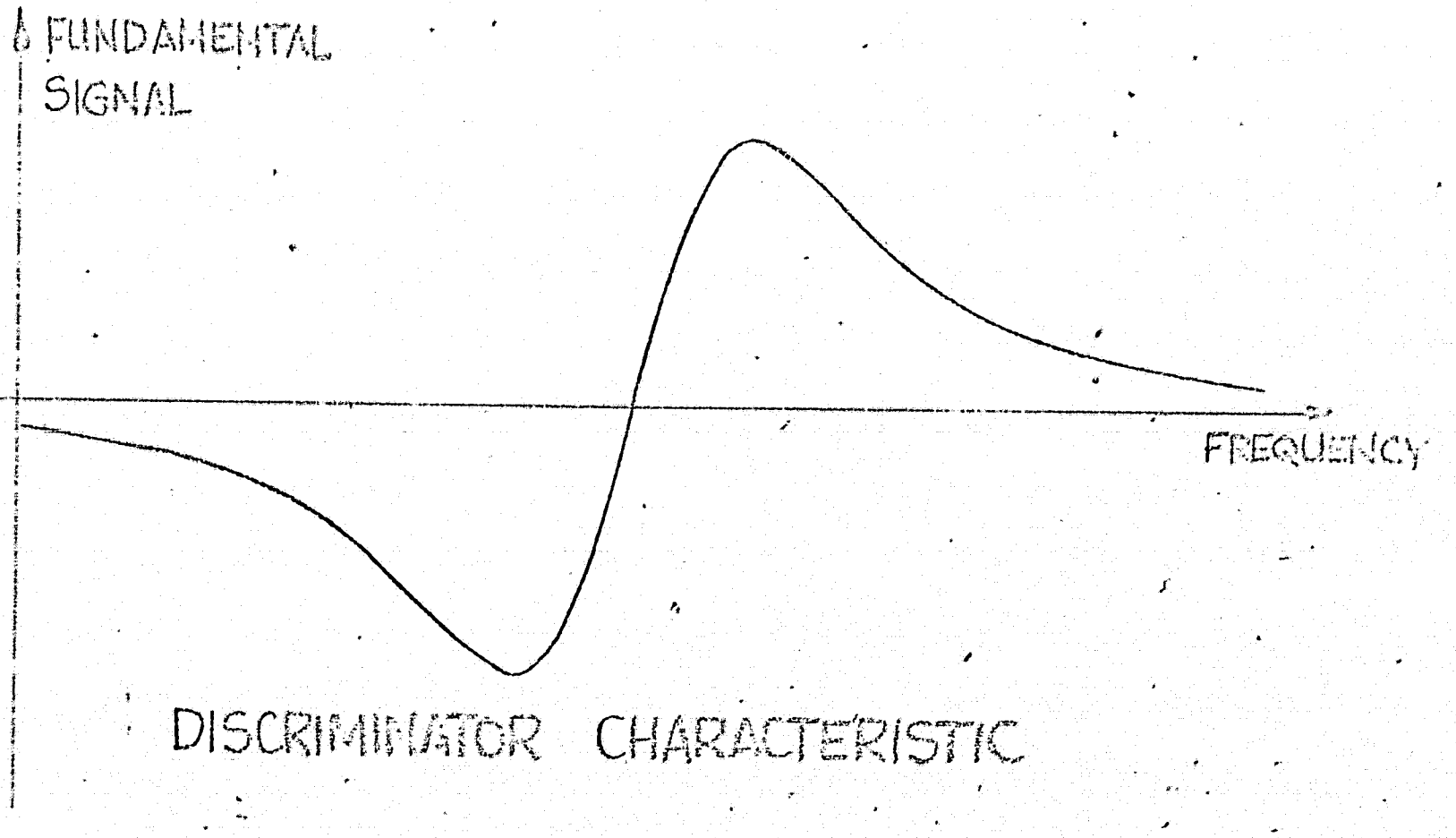

FUNDAMENTAL
SIGNAL
FREQUENCY
DISCRIMINATOR CHARACTERISTIC

FIG 4B

1.6 BASIC BLOCK DIAGRAM OF THE SPACECRAFT ATOMIC TIMING SYSTEM (SATS)

Figure 2995-9159-2D shows the basic block diagram of the SATS.

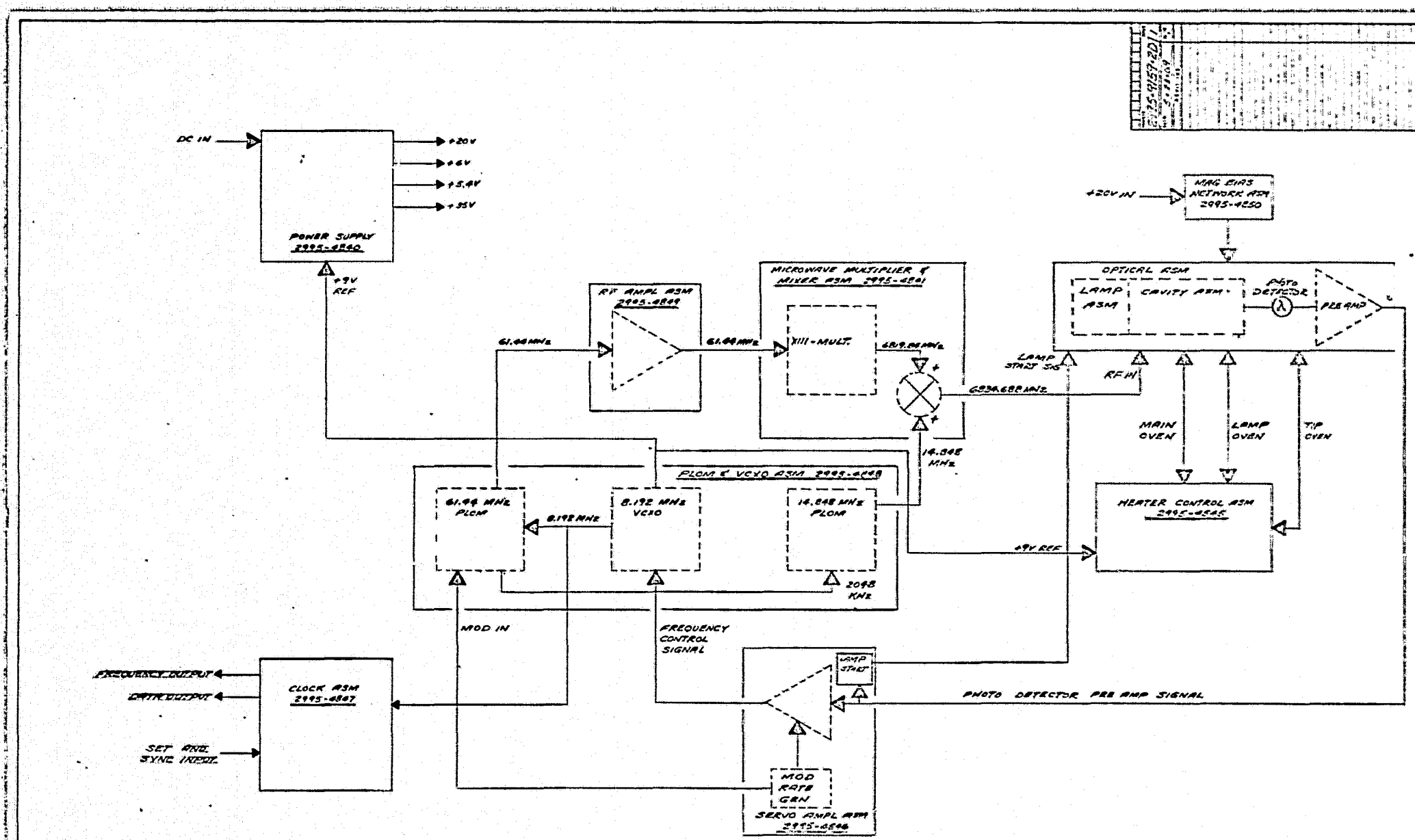
RF at the rubidium hyperfine transition frequency of 6834.688 MHz is derived from a Master Crystal Oscillator operating at 8.192 MHz and applied to the Optical Package. The Optical Package functions as a discriminator, producing an error signal which is processed by the servo amplifier to lock the frequency of the Master Crystal Oscillator to the rubidium resonance. The 8.192-MHz Master Crystal Oscillator is therefore controlled or "steered" by the highly stable atomic resonance and provides drive to the digital clock and thence the SATS output circuits.

Synthesis of the microwave drive used to excite the atomic transition begins by generating signals at 61.44 MHz and 14.848 MHz. These two signals are produced by Phase-Locked Crystal Oscillator Multiplier (PLOM) circuits whose frequencies are related to the 8.192-MHz Master Crystal Oscillator by the ratios (15/2) and (29/16), respectively. The signal at 61.44 MHz is then multiplied in frequency by a factor of 111 to produce a signal at 6819.84 MHz. This signal is mixed with the output of the 14.848 MHz PLOM, producing an upper sideband component at the desired rubidium transition frequency of 6834.688 MHz.

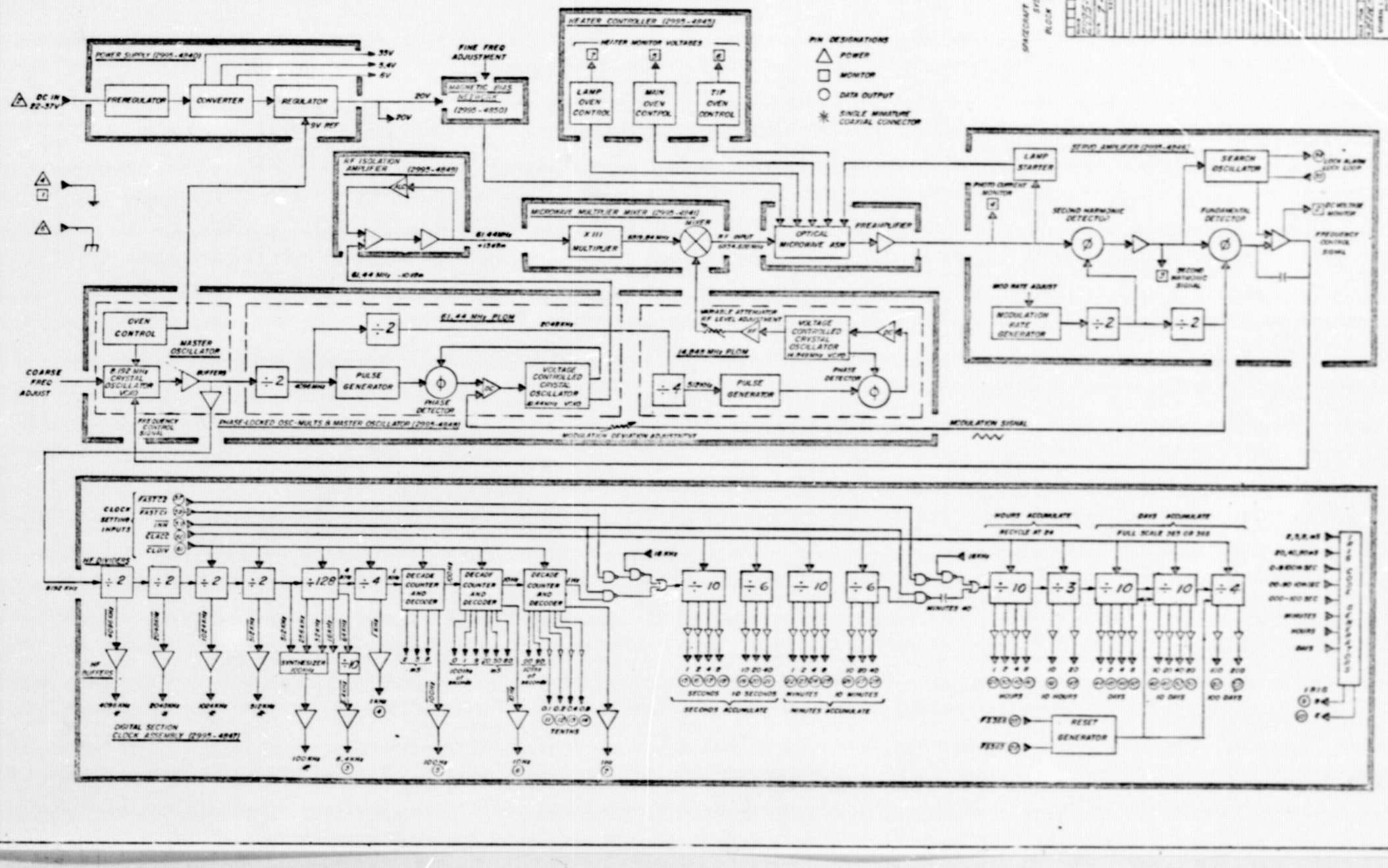
Other blocks of the SATS include a heater controller to maintain ovens in the Optical Package at the required operating temperatures; a magnetic field bias network for fine-frequency adjustment; and a power supply to serve the various circuits. Each SATS block or module is described in detail in the next section of this report.

A more detailed block diagram of the complete SATS is included as print 2995-9159-2DA/1. This print shows all of the available electrical signals

from the unit. A photograph of the complete SATS-1 is included as Figure 6. The view shown is prior to final topping-off of the potting compound and attaching the side cover plate.


DC IN
POWER SUPPLY
2995-4240
+20V
+6V
+5.4V
+35V
+9V REF
+20V IN
MAG BIAS NETWORK ASM
2995-4250
OPTICAL ASM
LAMP ASM
CAVITY ASM
PHOTO DETECTOR
PRE AMP
RF AMPL ASM
2995-4849
61.44 MHz
X111 - MULT.
6839.688 MHz
MICROWAVE MULTIPLIER & MIXER ASM 2995-4841
LAMP START SIG
RF IN
14.848 MHz
MAIN OVEN
LAMP OVEN
TIP OVEN
PLCM & VCXO ASM 2995-4848
61.44 MHz PLCM
8.192 MHz
8.192 MHz VCXO
14.848 MHz PLCM
2048 KHz
+9V REF
HEATER CONTROL ASM
2995-4545
MOD IN
FREQUENCY CONTROL SIGNAL
FREQUENCY OUTPUT
DATE OUTPUT
SET AND SYNC INPUT
CLOCK ASM
2995-4867
LAMP START
PHOTO DETECTOR PRE AMP SIGNAL
MOD RATE GEN
SERVO AMPL ASM
2995-4846

SPACECRAFT ATOMIC HMNS SYSTEM
BLOCK DIAGRAM



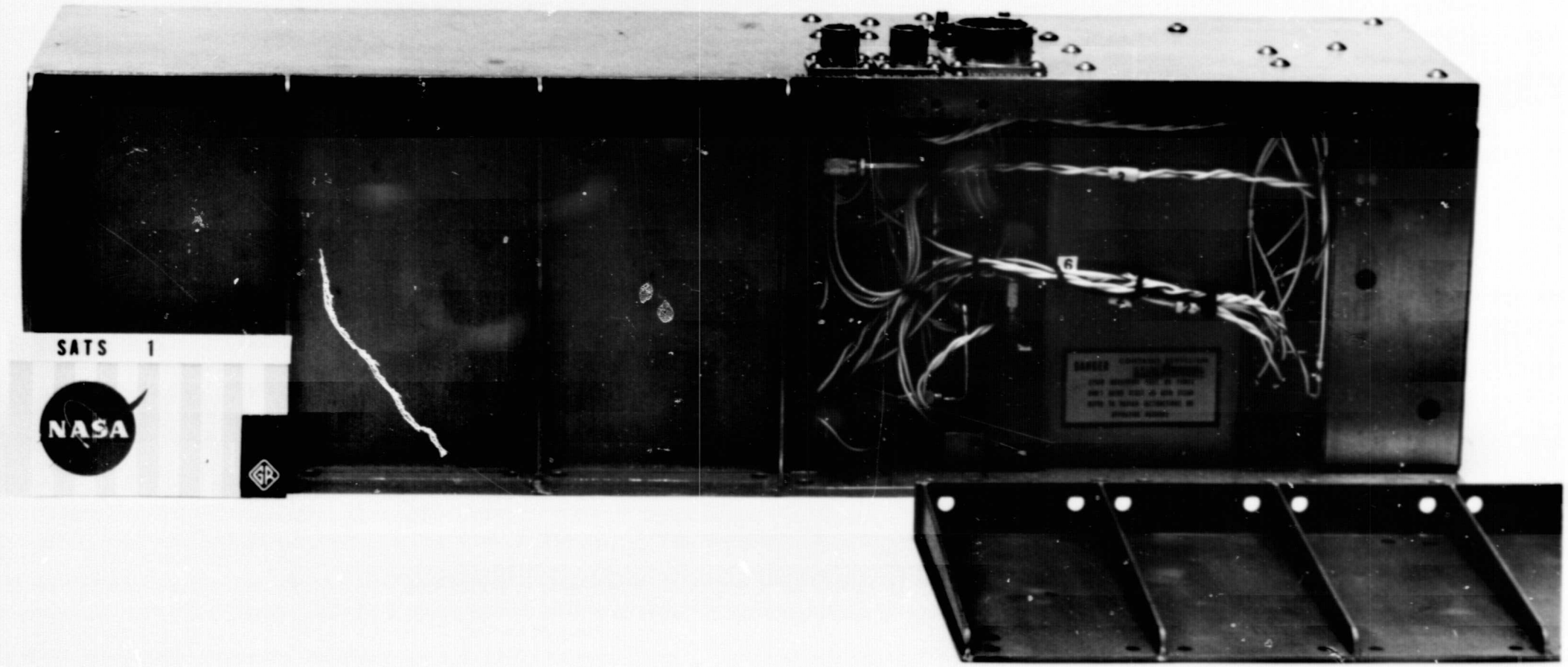


FIGURE 6

2.1 OPTICAL PACKAGE

A cutaway of the optical package is shown in Print 2995-9159-1. The Lamp Oscillator assembly is on the left. The Microwave cavity contains the absorption cell, the photodetector, and a link to feed in the microwave excitation signal via a coax cable. RF radiation through the apertures of the light beam is reduced by waveguide-beyond-cutoff sections at both ends of the cavity. The waveguide section on the right contains the photodetector, the one on the left (toward the lamp) holds the isotope filter cell. A tip sink, common to both the filter cell and the absorption cell, controls excess rubidium in both cells.

A bias-field winding, directly on the cavity, permits fine adjustment of frequency.

The cavity assembly is temperature-controlled at 75°C, the tip sink at 70°C. The cavity assembly contains both the filter cell and absorption cell.

As the isotope filter and the absorption cell operate at the same temperature, it is possible to obtain extremely low temperature coefficients by adjusting the gas filling of the absorption cell to result in a temperature coefficient equal and of opposite sign to that of the isotope filter.

The isotope filter has a temperature coefficient of about $-2 \times 10^{-11}/°C$. The temperature coefficient of the absorption cells can be reproduced to better than $\pm 1 \times 10^{-11}/°C$ from design center, resulting in an overall temperature coefficient of less than $1 \times 10^{-11}/°C$ in magnitude. The lamp-oscillator assembly has a temperature coefficient of $+1 \times 10^{-11}/°C$.

The thermal losses of the optical package (the required heater power) are a major portion of the total power budget. These losses have been minimized by use of highly efficient thermal insulation. The main oven uses "Nopco H402" urethane foam of low density and the lamp oven uses "Emerson & Cuming type FPH" urethane foam. The choice of materials is dictated by the operating temperatures of the ovens. The H402 foam has excellent thermal insulating properties, but its

maximum operating temperature is about 100°C (long-term exposure). The FPH foam has higher thermal conductivity (more losses) but can be operated to about 150°C. The use of different materials is therefore justified on the basis of minimum losses consistent with the required operating temperature. The heater windings are bifilar (to reduce magnetic effects) and wound on anodized aluminum cylinders. This provides electrical insulation between heater windings and ground in addition to the high quality insulation on the wire itself, for highest reliability.

The temperature sensors are glass-enclosed thermistor beads attached to the heater cylinders by means of thermally conductive epoxy for a high degree of coupling between the sensor and the controlled environment.

Considerable thought has been given to potential hazards in case of failure of a temperature controller. Urethane foams, when exposed to excessive temperatures, decompose. This results in objectionable fumes and development of substantial quantities of gases. As the optical package is hermetically sealed, fumes are contained. However, should a very large quantity of gas develop, the pressure could possibly build up to the rupture point of the enclosure. No completely satisfactory solution has been found to date. The Main-Oven with its 75°C operating temperature has a larger margin of safety than the lamp oven. The available maximum Main-Heater power is not enough to heat the foam to the point where large quantities of gas develop. The Lamp-Oven, however, in case of controller failure, will cause this condition. The obvious solution is to provide overtemperature protection by a secondary control element. A bimetallic thermostat was considered first but ruled out because of unpredictable performance under vibration (at least for the small size device required). The decision was made to install a fusible link in the Lamp-Oven. A device was selected, designed to operate reliably, under shock and vibration. This fusible link failed to disconnect, in one experiment, after exposure to over-temperature due

to solder bridging between the contacts, and the present design omits this link. In view of the possibility of gas development, the optical package was pressure tested. No deformation was noted at 45 PSIG. It is now felt that rupture cannot occur, even with failure of all temperature controllers so that fumes and gases are contained safely.

Magnetic Effects:

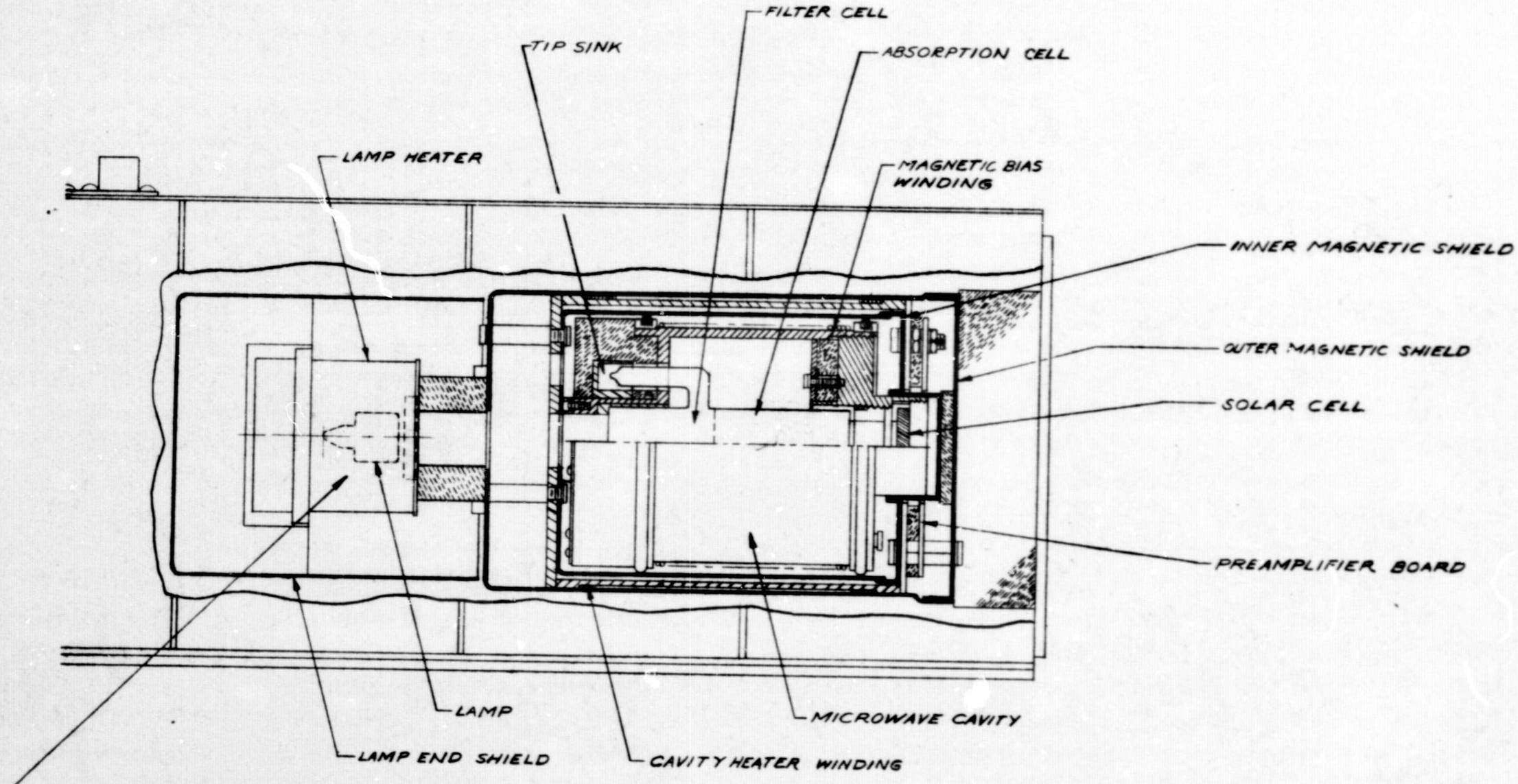
The frequency of the rubidium transition is magnetic field dependent

$$\Delta f = 573\ H^2$$

where Δf is the offset (in Hz) from the undisturbed transition frequency and H is the axial field (in Gauss).

Two Mu-metal shields reduce the effects of external fields to a few parts in 10^{11} per Gauss, considered consistent with the overall error budget for the SATS. At the cost of additional weight (~1 lb) a third shield could make this effect negligible.

The magnetic dependence of the frequency is used to provide a frequency adjustment of a few parts in 10^9 by varying the DC current through a bias winding on the cavity.



2995-9159-1

OPTICAL PACKAGE CUTAWAY

2.1.1 LAMP OSCILLATOR

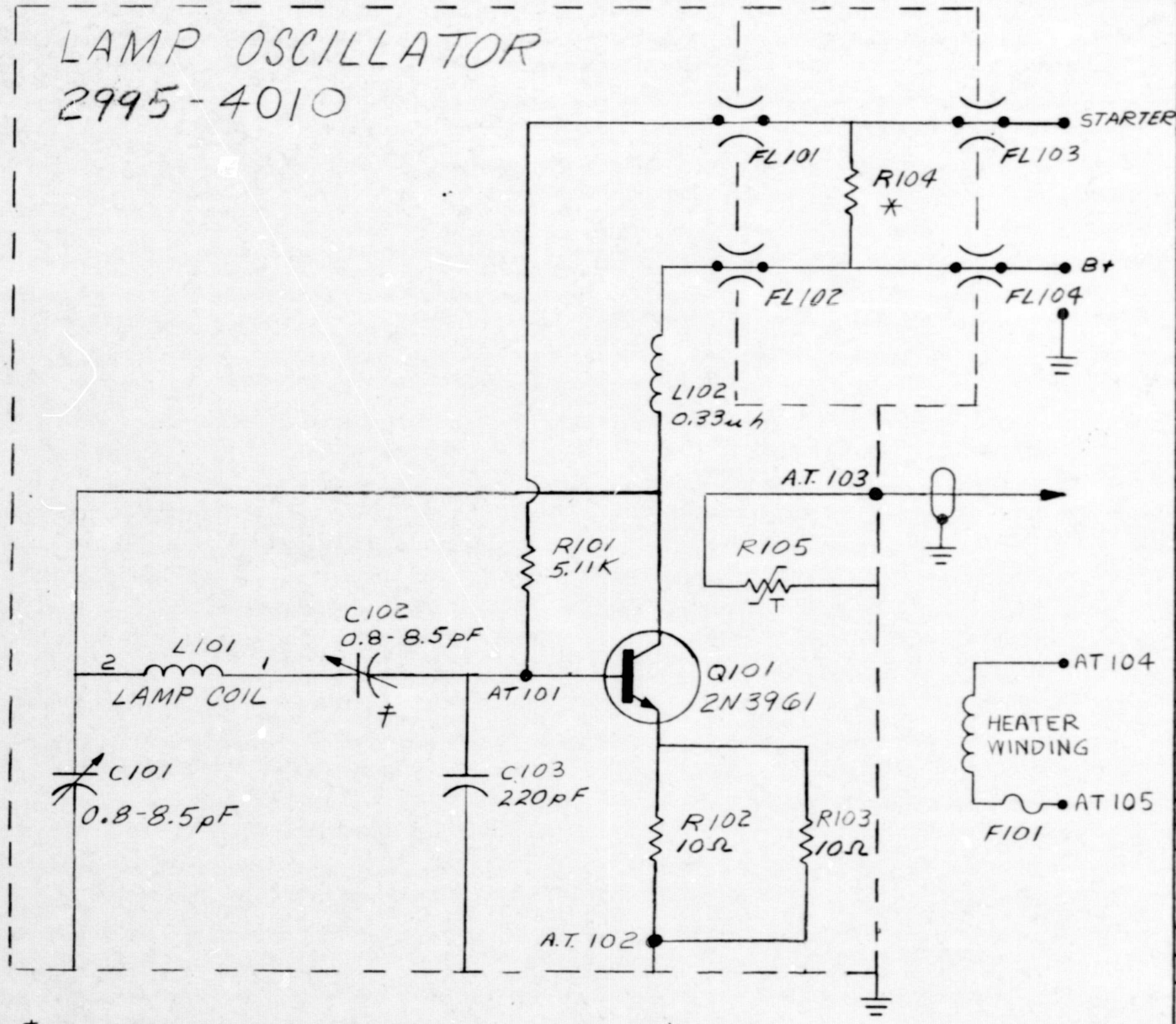
The light source for the optical pumping is an electrodeless, gaseous-discharge, bulb containing a small quantity of rubidium isotope 87 and some krypton gas. The discharge is excited by an RF power oscillator running at about 95 MHz. A diagram of the oscillator is shown in Print 2995-4842-2 DA/1. High-Q and series tuning provide a high RF voltage across the lamp coil (L101). Under operating condition, transistor bias is provided through R101 in series with R104. R104 is selected in test to set the DC current to approximately 55 mA. To start the lamp, extra bias is applied through the starter lead.

The entire assembly is temperature-controlled at approximately 122° C. During warmup of the lamp oven, the gaseous discharge undergoes a number of mode changes. At low temperature (room temperature) the vapor pressure of rubidium is very low and the light emission spectrum is essentially that of the krypton gas. Under normal operating conditions, the spectrum is predominantly that of rubidium, as rubidium has lower ionization potential than krypton.

Between these two well-defined modes there exists a transition phase where rapid oscillations between the two modes occur.

The location of the lamp oscillator assembly inside the optical package is shown in Print 2995-9159-1. A photograph of the assembly is shown as Figure 7.

LAMP OSCILLATOR
2995-4010



† ADJ. FOR NOMINAL FREQUENCY OF 95 MHz

* DETERMINED BY LAB NOMINAL ≈ 30 KΩ

NUMBER	ISSUE
2995-4842-2DA	1
DATE: 12 - 31 - 68	ISSUE 1

REVISIONS

SCALE ~	FIRST USED ON	
DR. JRS	CH.	APP.

GENERAL RADIO COMPANY
BOLTON PLANT
BOLTON MASS U S A

NUMBER	ISSUE
2995-4842-2DA	1

FORM 8101A

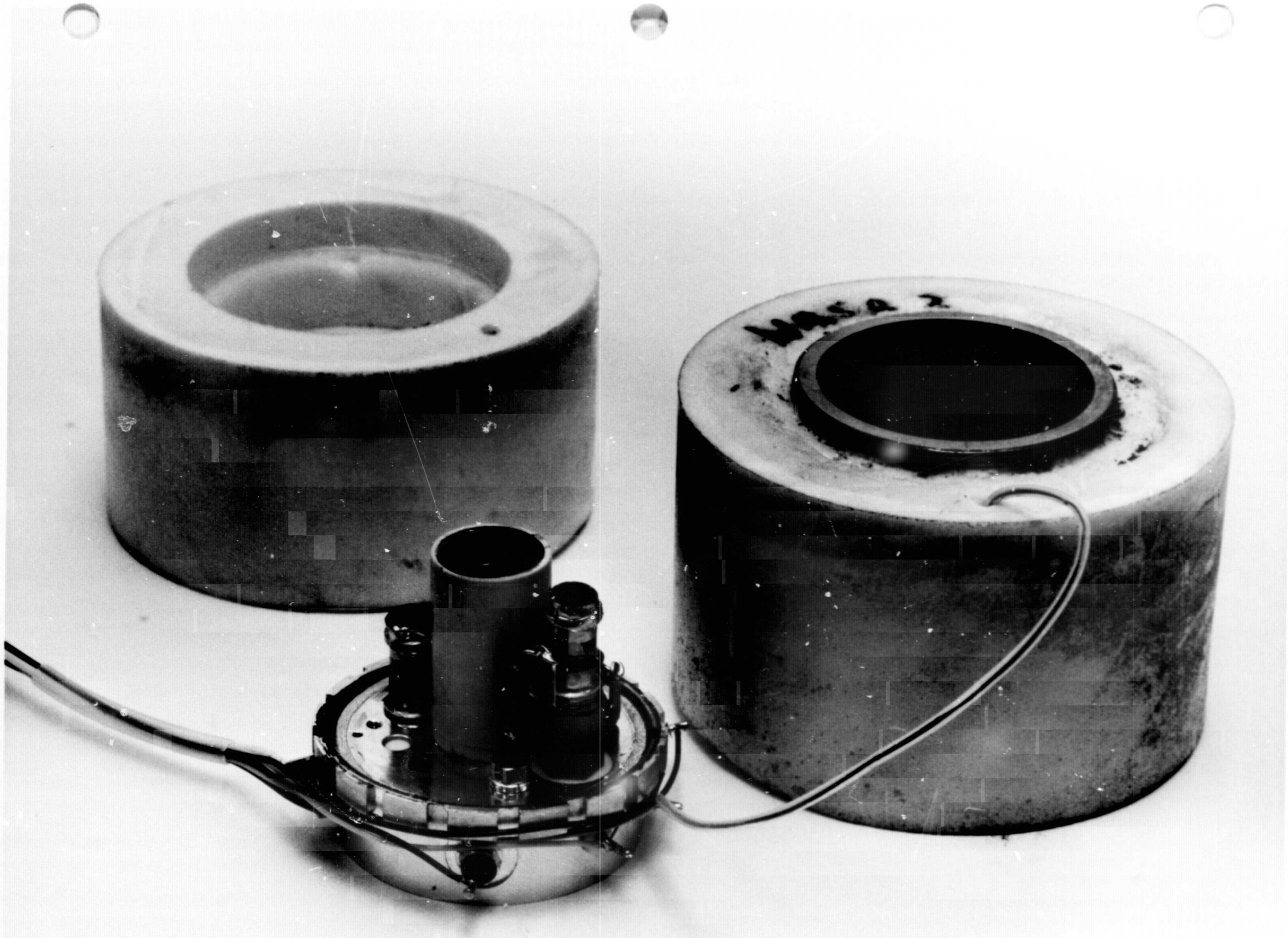


FIGURE 7

2.1.2 PHOTODETECTOR AND PREAMPLIFIER

The photodetector is a silicon photo diode (solar cell) made from 1000-ohm material. The high resistivity material was chosen to obtain low capacitance. Print 2995-9159-2 DD/1 is a diagram of the preamplifier. The photodetector looks into a low impedance load and the voltage across the photodetector is always less than 10 mV. The feedback configuration of the monolythic operational amplifier IC-1 is such that input and output impedance are low and the transfer function is a transimpedance, i.e., assuming infinite open loop gain for the Op-Amp, the transimpedances are determined as follows:

$$\text{for DC} \qquad Z_T = R_1 + R_2$$

$$\text{for Modulation Signal} \qquad Z_T = \frac{R_1 R_2}{R_3 + R_6}$$

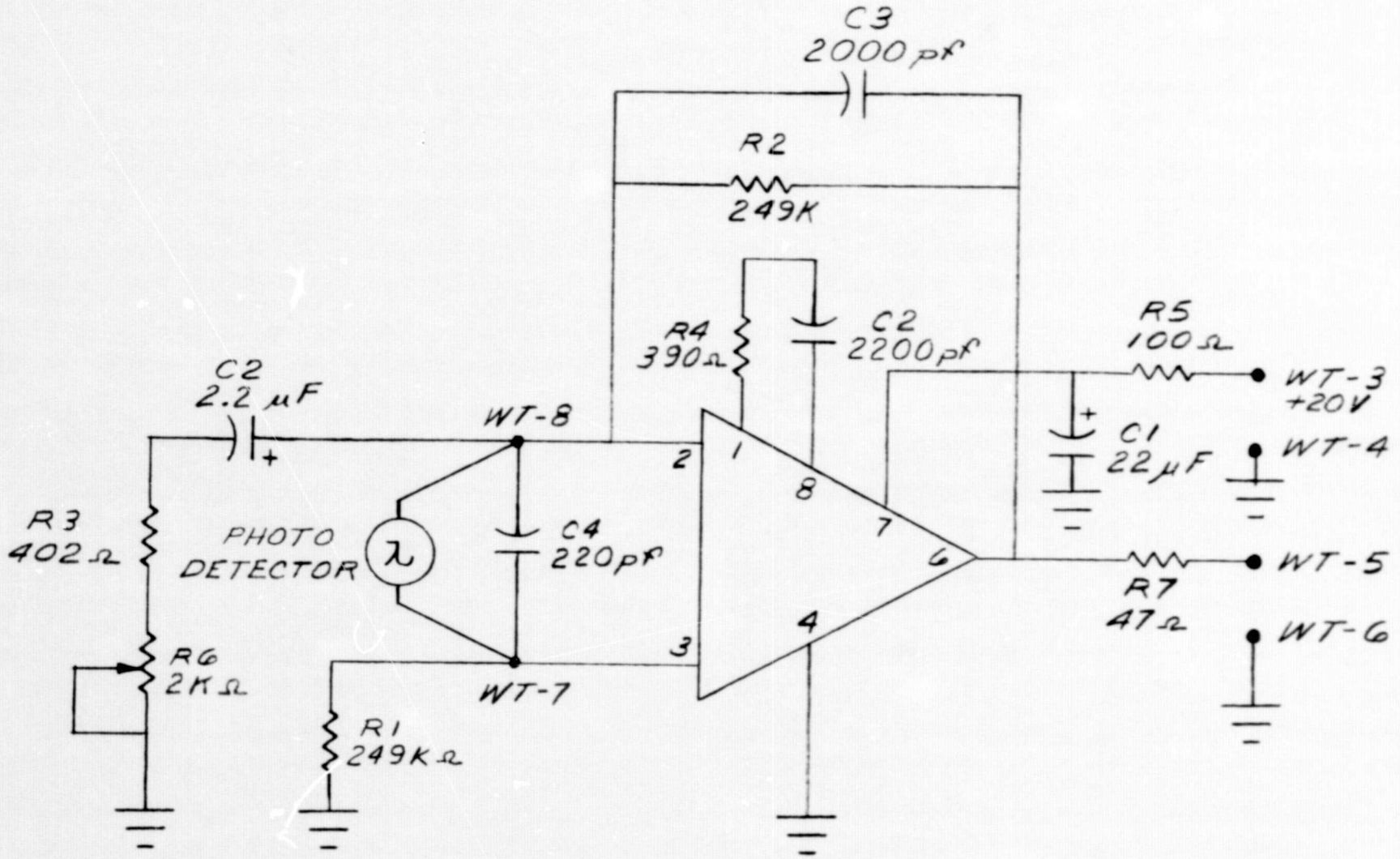
the frequency response is shaped by C_2 and C_3 to provide rolloff for low frequencies (low DC gain) and for high frequencies (low RF gain).
As the transimpedance for DC is 498 kΩ , a DC level of 10 V at the output terminal of the preamp corresponds to about 20 μA of photocurrent. The AC gain can be adjusted by R_6 and is set to produce approximately 2.5 mV rms of fundamental signal for a frequency error of 1×10^{-10}.

If the lamp is not started, there is no photocurrent and the DC output level of the preamp is near zero volts. Under proper operating conditions the level is between +10 and +20 volts. This DC level shift is used to activate the lamp starter (see Servo Amp) circuit.

The preamplifier is located between the inner and outer mu-metal shields.

Break-A-Way View of Optical Package

Figure 8 is a break-a-way photo of the Optical Package Components.



WIRING DIAGRAM FOR
PHOTODETECTOR PREAMPLIFIER

NUMBER	ISSUE
2995-9159-2DD	1
DATE: 12-9-69	ISSUE 1
REVISIONS	

SCALE — FIRST USED ON

DR. — CH. — APP.

GENERAL RADIO COMPANY
BOLTON PLANT
BOLTON MASS U S A

NUMBER	ISSUE
2995-9159-2DD	1

FORM 81013A

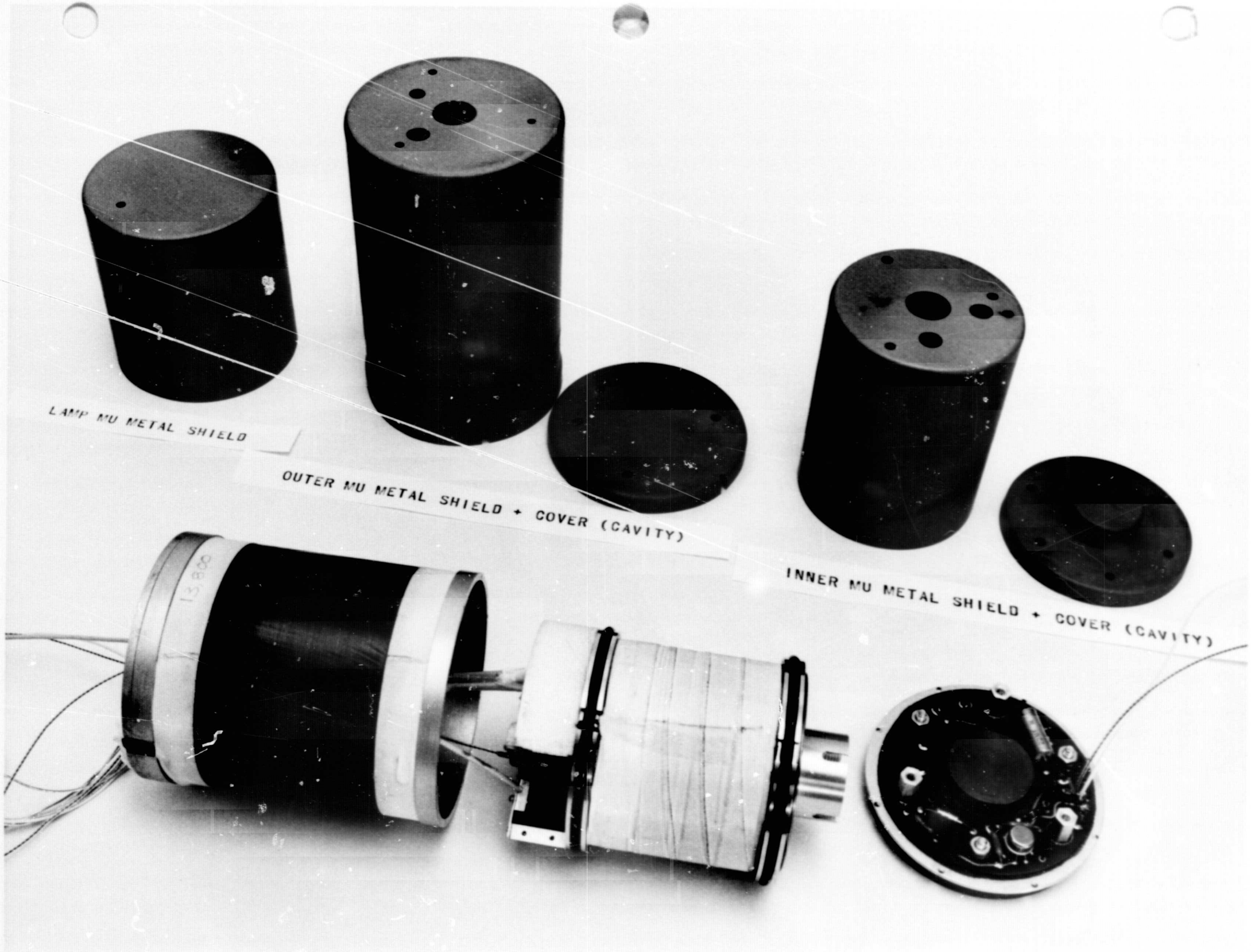

LAMP MU METAL SHIELD
OUTER MU METAL SHIELD + COVER (CAVITY)
INNER MU METAL SHIELD + COVER (CAVITY)

FIGURE 8

2.2 MASTER CRYSTAL OSCILLATOR AND PHASE-LOCKED-OSCILLATOR MULTIPLIERS

This module assembly, depicted in Print 2995-4848, consists of three sections: (1) the 8.192 MHz (VCXO) Master Crystal Oscillator, (2) the 61.44 MHz PLOM , and (3) the 14.848 MHz PLOM.

Each of these three submodules is discussed in the balance of this section of the report.

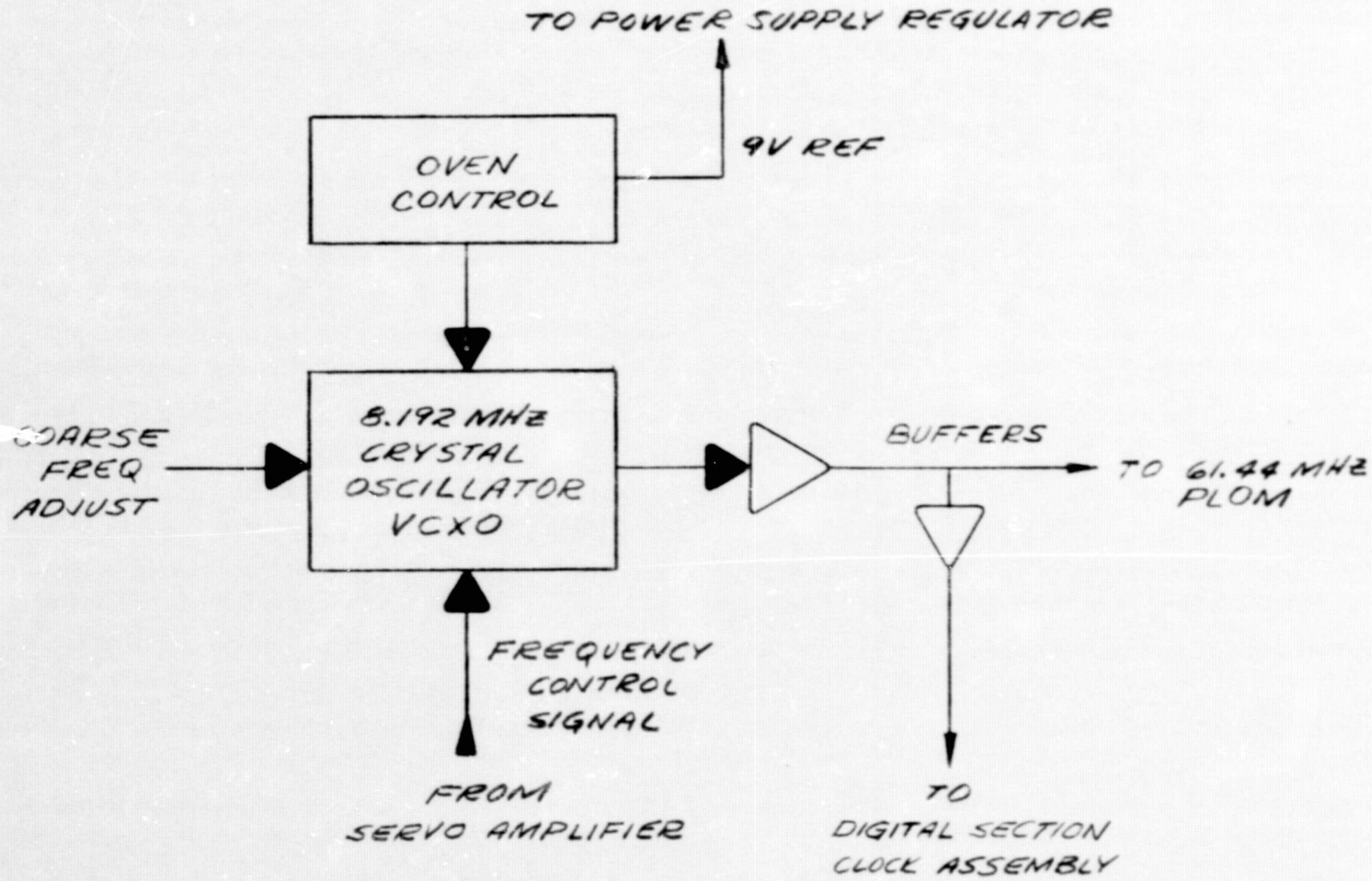
Photographs of the Master Crystal Oscillator, 61.44 MHz and 14.848 MHz PLOM's are shown as Figures 10 and 11. Print 2995-4848/2 depicts the physcial locations of the submodules.

2.2.1 8.192 MHz VCXO (MASTER CRYSTAL OSCILLATOR)

A proprietary General Radio 10 MHz Crystal Oscillator design used as a precision time-base oscillator in electronic counters served as the basis for this SATS component. A special 8.192 MHz quartz crystal, zener reference diode and temperature control thermistor are substituted for the equivalent parts of a General Radio standard unit for this SATS application.

The oscillator circuit is a Colpitt's configuration with a junction field-effect transistor as the active device. Both the quartz crystal and the oscillator circuit are inside an oven which is held at constant temperature by an internal proportional-oven control circuit. A 9-volt zener diode is also in the temperature-controlled environment and is used as the reference for the 20-volt power supply regulator. A three-stage buffer amplifier follows the crystal oscillator and provides the output from this unit.

A photograph of the Master Crystal Oscillator, during assembly, is shown as Figure 9.



2995-4848-2DA-1/1

MASTER OSCILLATOR

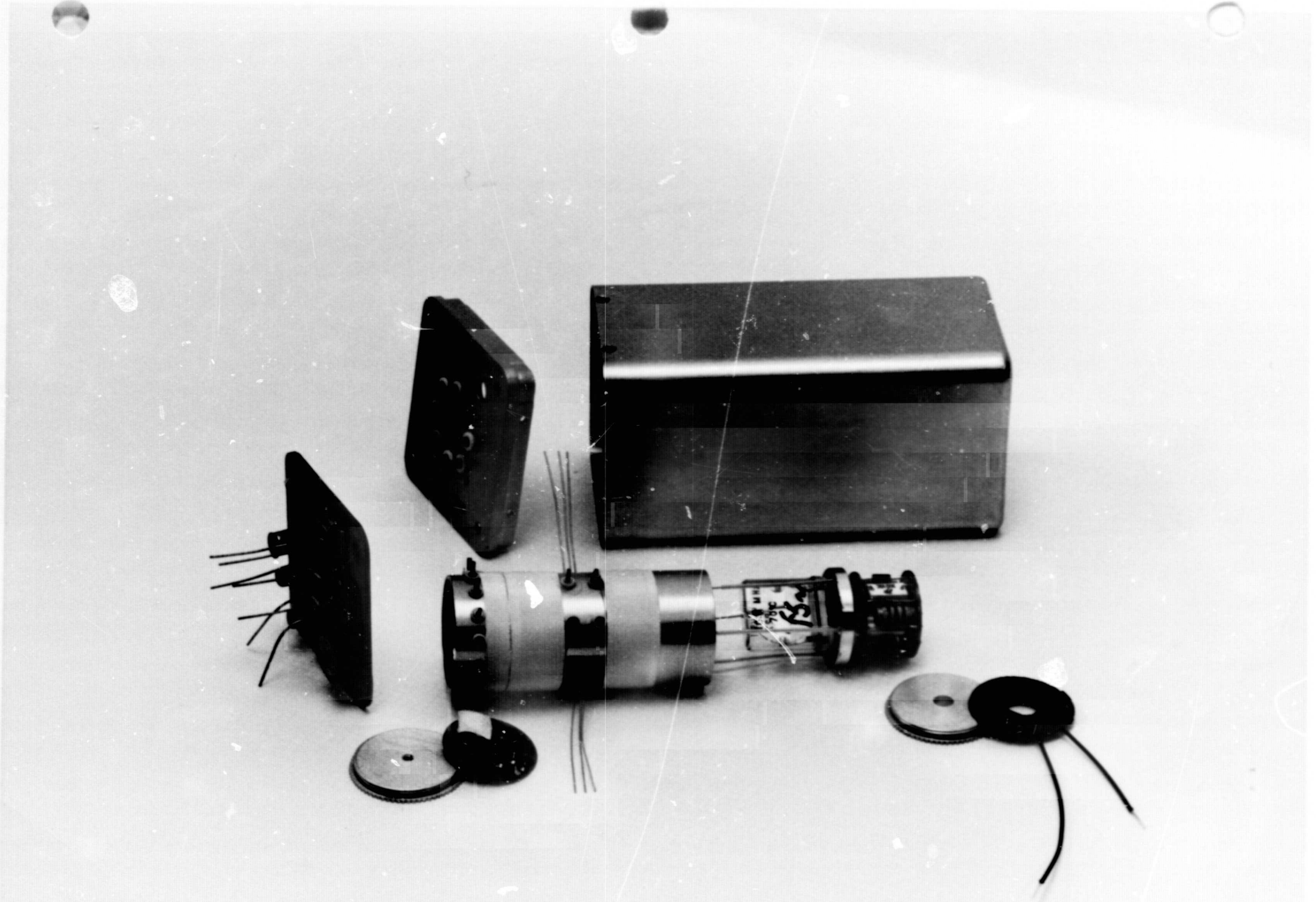


FIGURE 9

2.2.2 61.44 MHz PLOM

Introduction:

The 61.44 MHz PLOM (Phase-Locked-Oscillator Multiplier) performs two functions: (1) multiplication of 4096 kHz (one-half the 8.192 MHz input frequency) by a factor of 15 to produce 61.44 MHz drive for the Microwave Multiplier-Mixer; (2) modulation of the 61.44 MHz output to provide an error signal for the servo-loop. These two functions are accomplished as shown in the block diagram of Print 2995-4848-2DA2/1.

Frequency Multiplication:

A signal at the rubidium hyperfine transition frequency must be produced by multiplication and synthesis of the crystal oscillator output at 8.192 MHz. The first portion of this frequency multiplication is accomplished by phase-locking a voltage-controlled crystal oscillator (VCXO) operating at 61.44 MHz to the 15th harmonic of 4096 kHz. A sampling-type phase detector is used and the phase-lock loop has wide bandwidth ($\approx$ 5 kHz) as required for best spectral purity of the 61.44 MHz output. The lock range is sufficiently wide (±50 ppm) to maintain lock as the oscillator free-running frequency changes with temperature, aging, etc.

Frequency Modulation:

Low distortion frequency modulation is an essential requirement of any rubidium frequency standard. Even-order (2nd, 4th, etc.) harmonic distortion of the fm applied to the rf which excites the rubidium hyperfine transition shifts the center of the rf spectrum causing a frequency offset from the center of the rubidium resonance. Second harmonic distortion at 600 Hz must be down about 60 dB (0.1%) if the offset is to be $< 1 \times 10^{-11}$.

A phase-lock loop can serve as a low distortion phase modulator. A triangular wave phase modulation signal injected at the input of the lock loop dc amplifier (see Print 2995-4848-2DA2/1) will produce square-wave frequency modulation of the rf output. Furthermore, the closed loop provides negative feedback which serves to linearize the frequency versus control voltage characteristic of the VCXO and thus reduces modulation distortion. The resulting transfer function of the modulator is the reciprocal of the phase-detector transfer function. In order to maintain constant fm deviation it is therefore necessary to keep the rf input to the phase detector constant and desirable to provide high dc loop gain in order to minimize changes in the phase detector operating point.

Circuit Description:

These requirements are met by the circuit shown in Print 2995-4880-2D and described as follows:

(1) Digital Divider (Dual Flip-Flop):

Input from a transformer secondary winding in the 8.192 MHz crystal oscillator is applied through the R1, C1 network to the first flip-flop clock terminal. This network provides self-bias designed to produce a dc level between the "0" and "1" logic thresholds for optimum triggering of the flip-flop from a sine-wave input signal amplitude of about 3 volts peak to peak.

The 4096 kHz flip-flop output drives the strobe pulse generator and the second flip-flop.

The 2048 kHz output from the second flip-flop is used to drive the 14.848 MHz PLOM.

(2) Strobe Pulse Generator:

A fast strobe pulse for the sampling phase detector is produced by a step-recovery diode, CR4, and this portion of the circuit.

4096 kHz drive from the first flip-flop is applied through the CR1, CR2, R2, R3, C3 network to transistor Q1. This network simulates a DTL logic interface. When the flip-flop is in the "0" state (low) Q1 is off and a forward current of 10 mA flows through CR4 as established by R4 and the CR5 zener voltage. When the flip-flop is triggered to the "1" state (high) Q1 is turned on and diverts the current from CR4. Since the anode of CR3 goes nearly to ground, CR4 is actually reverse biased. Forward current will continue to flow through CR4 for a short time, however, until the charge stored in its depletion region is swept out. The diode then switches abruptly to the off state, producing a negative pulse of about 7 volts amplitude and 2-ns duration at its anode. Inductor L1 keeps the current through Q1 constant during this interval, preventing the pulse from being absorbed by Q1, and capacitor C5 couples the pulse to the primary of T1. The strobe pulse generator thus produces a pulse with a duration only a fraction of an rf carrier period at 61.44 MHz (16 ns) as required by the phase detector.

(3) Phase Detector:

The strobe pulse is applied to the 4-diode (CR7-CR10) sampling phase detector through T1 and capacitors C6 and C7. Diode CR6 clips off any undesired positive overshoot on the pulse.

The instantaneous 61.44 MHz signal amplitude is applied through the sampling detector to the holding capacitor C9 during the strobe pulse interval when the sampling diodes are turned on. The charging time constant is sufficiently short to allow C9 to charge to about 80% of the rf amplitude during a 2-ns strobe pulse.

Reverse bias is applied to the detector diodes to insure the bridge will not pass rf without the presence of a strobe pulse. This is accomplished by the voltage drop across R6 which is about 3 volts.

The holding time constant of the sampling detector is determined by C9 and R8 (the dc amplifier input current is negligible) and is very long compared with a 4096 kHz carrier cycle as is desired for high detector efficiency.

The R9, C11 network isolates the dc amplifier from the phase detector strobe pulse while C8 and T2 accomplish the same thing for the crystal oscillator.

(4) DC Amplifier:

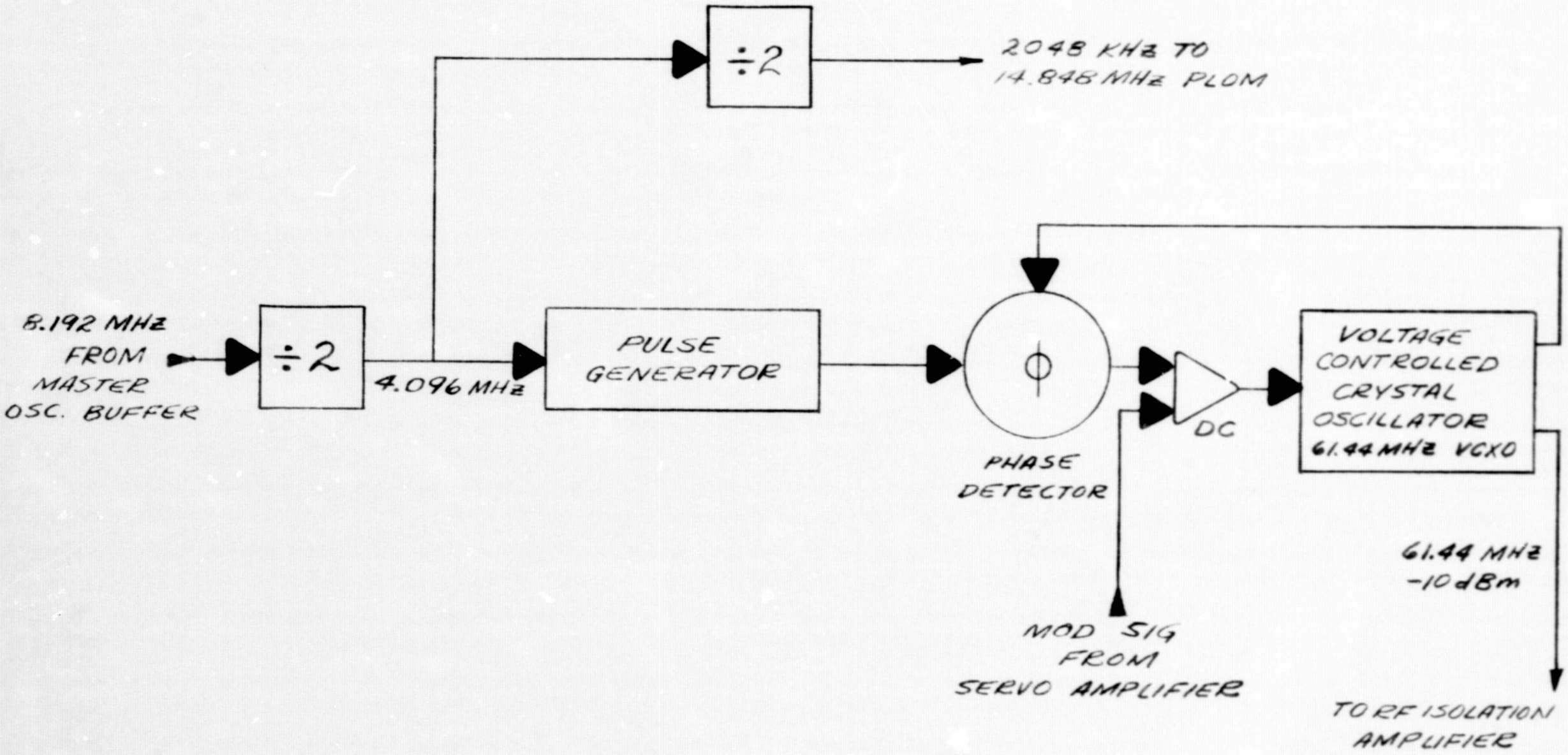
The dc amplifier is a straightforward application of a monolithic integrated circuit operational amplifier. The amplifier is operated without dc feedback since the highest dc loop gain is desirable for modulator stability. The R11, C14 network together with R10 establishes the ac gain of the amplifier. The triangular-wave modulation signal is applied through R12 and the fm deviation adjusted with R10.

(5) Crystal Oscillator:

The 61.44 MHz crystal oscillator is a configuration with noninverting gain provided by a grounded-base stage and a positive feedback path from the secondary of transformer T3 through quartz crystal X1 to the emitter of Q2. Coarse adjustment of oscillator frequency is provided by L3 while the two series connected variable capacitance diodes, CR11 and CR12, provide voltage control of frequency over a range of about 100 ppm. Inductor L2 is used to tune out the static capacitance of the quartz crystal.

(6) ALC Amplifier:

Constant oscillator output level, required primarily to keep the fm deviation constant, is provided by the ALC amplifier. Diode CR13 detects the rf output level and the ALC amplifier varies the oscillator bias as required to maintain constant output level.



2995-4848-20A-2/1

61.44 MHz PLOM

NOTE UNLESS SPECIFIED

1. POSITION OF ROTARY SWITCHES SHOWN COUNTERCLOCKWISE.
2. CONTACT NUMBERING OF SWITCHES EXPLAINED ON SEPARATE SHEET SUPPLIED IN INSTRUCTION BOOK.
3. REFER TO SERVICE NOTES IN INSTRUCTION BOOK FOR VOLTAGES APPEARING ON DIAGRAM.
4. RESISTORS 1/2 WATT
5. RESISTANCE IN OHMS K = 1000 OHMS M = 1 MEGOHM
6. CAPACITANCE VALUES ONE AND OVER IN PICOFARADS, LESS THAN ONE IN MICROFARADS.
7. ○ KNOB CONTROL
8. ⊗ SCREWDRIVER CONTROL
9. AT - ANCHOR TERMINAL
10. TP - TEST POINT

2995-4860-20/2

STROBE PULSE GENERATOR

PHASE DETECTOR

D.C. AMPLIFIER

R2 4.7K
R4 1K
R5 3.01K
R26 100
CR1
CR2
CR3
CR4
CR5 10V
CR6
CR7
CR8
CR9
CR10
L1 .15μH
Q1
T1
T2
C1 .01
C2 4.7μF
C3 100
C4 .01
C5 43
C6 100
C7 100
C8 30
C9 33
C10 2.2μF
C11 33
C12 33
C13 6.8μF 35V
C20 1μF 35V
R1 1K
R3 1K
R6 1K
BAL ADJ
R7 3.01K
R22 100
R8 100K
R9 1K
R10 20K
DEV ADJ
R11 330K
R12 330K
R13 10K
R28 100K
IC2
WT-11 LOOP METER OUT
HAND WIRED LEAD FROM RESISTOR TERMINAL TO TERMINAL 11
+30V WT-7
VCXO PIN-6
WT-10 (SERVO)
WT-15
WT-8
WT-12 (SERVO) (MODULATION SIGNAL)
WT-6
WT-9 (SERVO)

XTAL OSCILLATOR

ALC AMPLIFIER

DUAL FF IC1

4.096 kHz OUT WT-3
WT-4 PLOM ENA
WT-5 (2048 CLOCK)
WT-2 (1.4MHz)
WT-6 RESET IN
WT-1 (1.4MHz)
VCXO PIN-3
VCXO PIN-4 (1.102 MHz)

C15 330
C16 330
C17 10
C18 330
C19 100
C21 330
C22 2.2μF
C30 1μF 35V
R14 100
R15 4.7K
R16 820
R17 100K
R18 100K
R19 3.3M
R20 240K
R21 47
R22 100K
R23 15K
R24 220
R25 6.2
R29 10K
R30 1K
Q2
Q3
Q4
L2
L3 .82μH
X1 61.44 MHz
CR11
CR12
CR13
WT-9 ALC METER OUT
WT-10 RF AMP OUT
WT-17 RF GND
C20 .001

* VALUE TO BE DETERMINED IN TEST

61.44 MHz PLOM WIRING DIAGRAM

2.2.3 14.848 MHz PLOM

Introduction

The 14.848 MHz PLOM (Phase Locked Oscillator Multiplier) accepts an input signal at 2048 kHz from the 61.44 MHz PLOM board, divides it by a factor of four to 512 kHz, then multiplies this frequency by 29 to produce a signal at 14.848 MHz which drives the i-f port of the Microwave Multiplier-Mixer. The frequency multiplication is accomplished by phase locking a voltage-controlled crystal oscillator (VCXO) operating at 14.848 MHz to the 29th harmonic of 512 kHz. The crystal oscillator drives a temperature-compensated cascade amplifier circuit. A variable attenuator network follows the amplifier and provides an adjustable rf level to the microwave mixer. A block diagram of the 14.848 MHz PLOM is included in Print 2995-4848-2DA3/1.

Circuit Description:

The schematic circuit diagram of the 14.848 MHz PLOM is Print 2995-4881-2D/2; the unit operates as follows:

(1) Strobe Pulse Generator:

The dual flip-flop IC1 accepts a 2048 kHz T^2L square-wave signal at 512 kHz. This signal is coupled by C2 to the base of Q1, the strobe pulse generator stage. Transistor Q1 is turned on during the positive transistions of the 512 kHz signal. This produces a current pulse through transformer T1 which turns on diodes CR2 and CR3 for an interval of about 15 ns.

(2) Phase Detector:

RF from the crystal oscillator is coupled through C5 and C6 into the sampling phase detector. During a strobe pulse the holding capacitor C7 is charged to the instantaneous amplitude of the rf signal through CR2 and CR3. The strobe pulse duration is short compared with the period of the 14.848 MHz signal, and the C7 charging time constant is shorter than the strobe pulse duration, the conditions required for good detector efficiency. In addition, the

C7 holding time constant is long compared with a period of the 512 kHz input frequency. Reverse bias of the sampling diodes is provided by the voltage drop across R4 to prevent rf feedthrough when no strobe pulse is present.

(3) DC Amplifier:

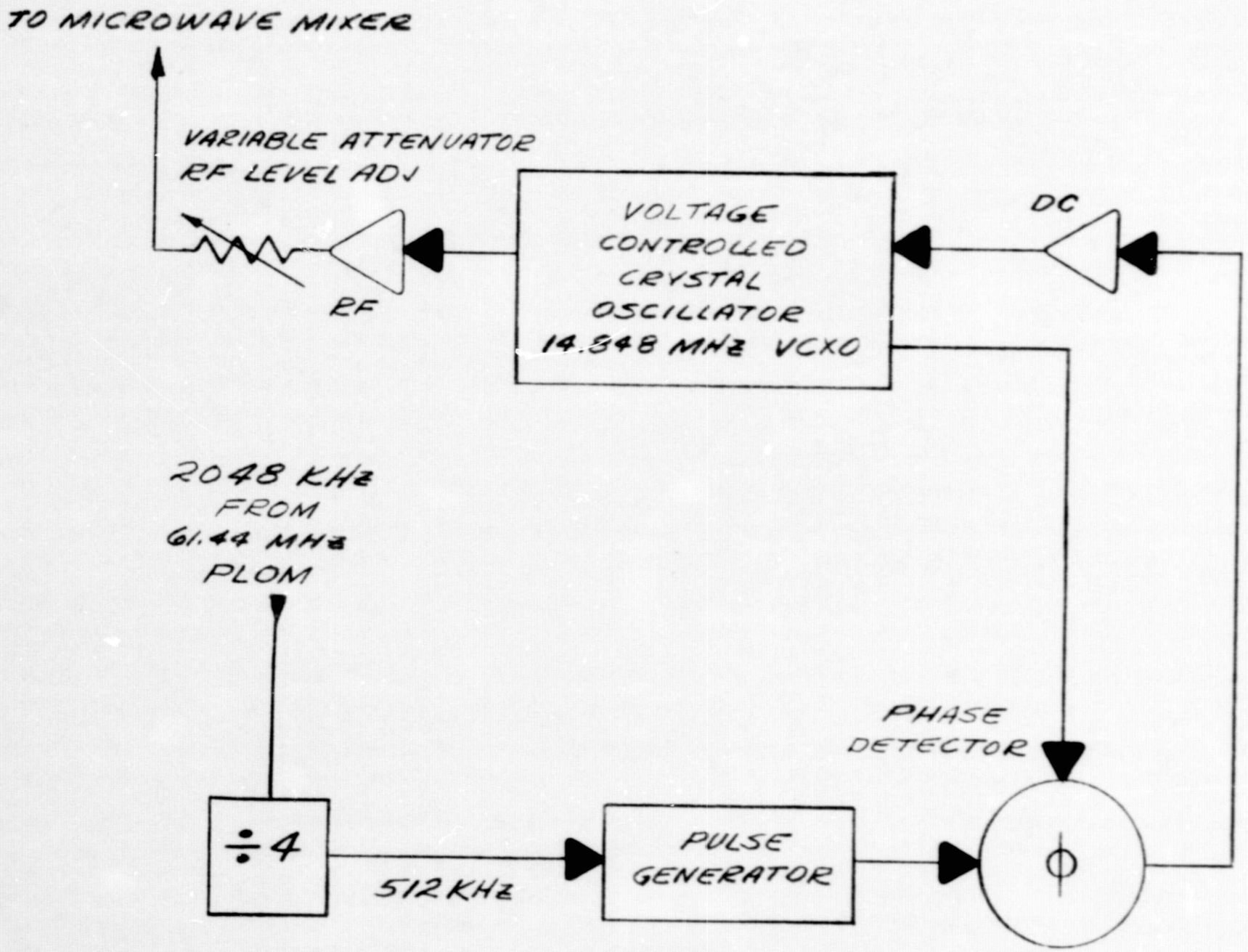
The dc amplifier circuit is a straightforward application of a monolythic IC operational amplifier.

(4) Crystal Oscillator:

The 14.848 MHz crystal oscillator is a Colpitt's configuration with the Q2 stage providing inverting transconductance determined by R14, with C12, C13 and the crystal providing the 180° phase shift required for positive feedback. Inductor L1 prevents oscillation at the crystal's fundamental mode, diode CR5 provides amplitude limiting and variable capacitance diode CR4 permits voltage control of frequency. Transistor Q3 is an emitter follower which provides isolation between the oscillator and phase detector.

(5) RF Amplifier:

Transistors Q4 and Q5 form a cascode amplifier which produces an output of about +12 dBm. Diodes CR6 and CR7 serve to temperature-compensate the output power. Resistors R23, R24, and R25 form variable attenuator network which adjust the signal applied to the 14.848 MHz input of the mixer section of the Microwave Multiplier-Mixer.



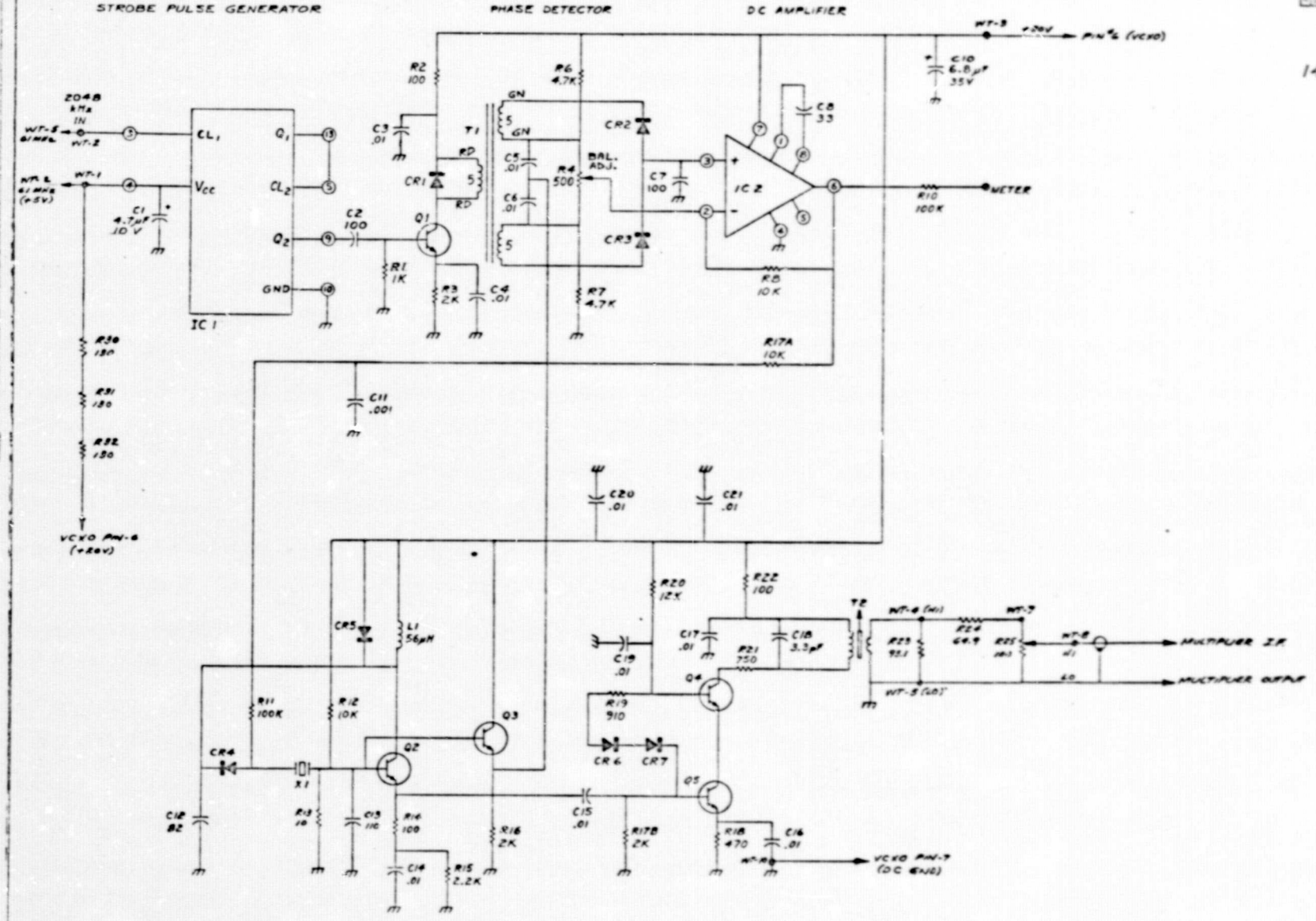
2995-4848-2DA-3/1

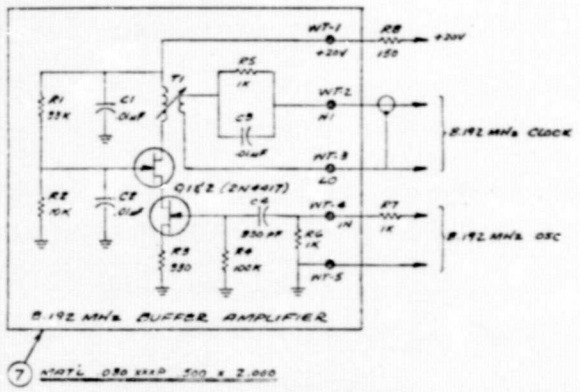
14.848 MHz PLOM

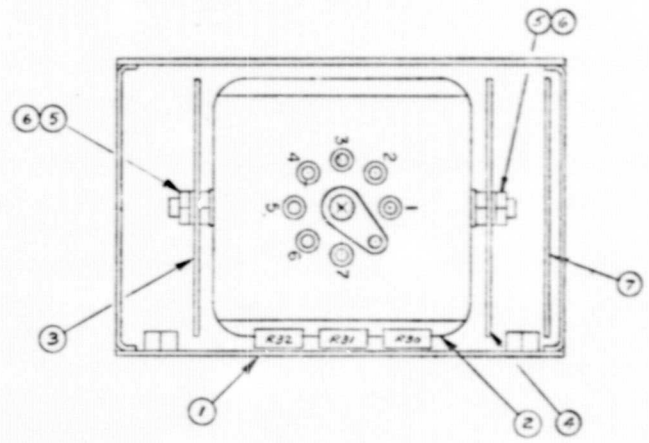
NOTE UNLESS SPECIFIED

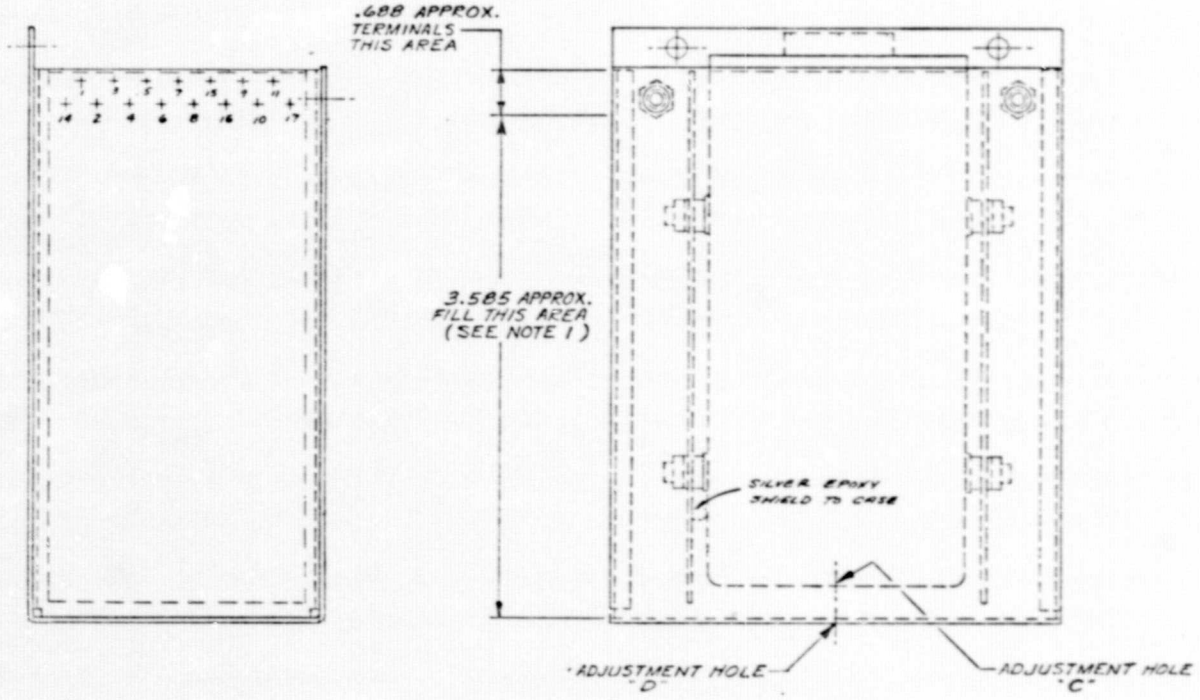
1. POSITION OF ROTARY SWITCHES SHOWN COUNTERCLOCKWISE.
2. CONTACT NUMBERING OF SWITCHES EXPLAINED ON SEPARATE SHEET SUPPLIED IN INSTRUCTION BOOK.
3. REFER TO SERVICE NOTES IN INSTRUCTION BOOK FOR VOLTAGES APPEARING ON DIAGRAM.
4. RESISTORS 1/2 WATT.
5. RESISTANCE IN OHMS K = 1000 OHMS M = 1 MEGOHM
6. CAPACITANCE VALUES LESS THAN ONE IN MICROFARADS.
7. KNOB CONTROL
8. SCREWDRIVER CONTROL
9. AT = ANCHOR TERMINAL
10. TP = TEST POINT

14.848 MHz FLOM WIRING DIAGRAM









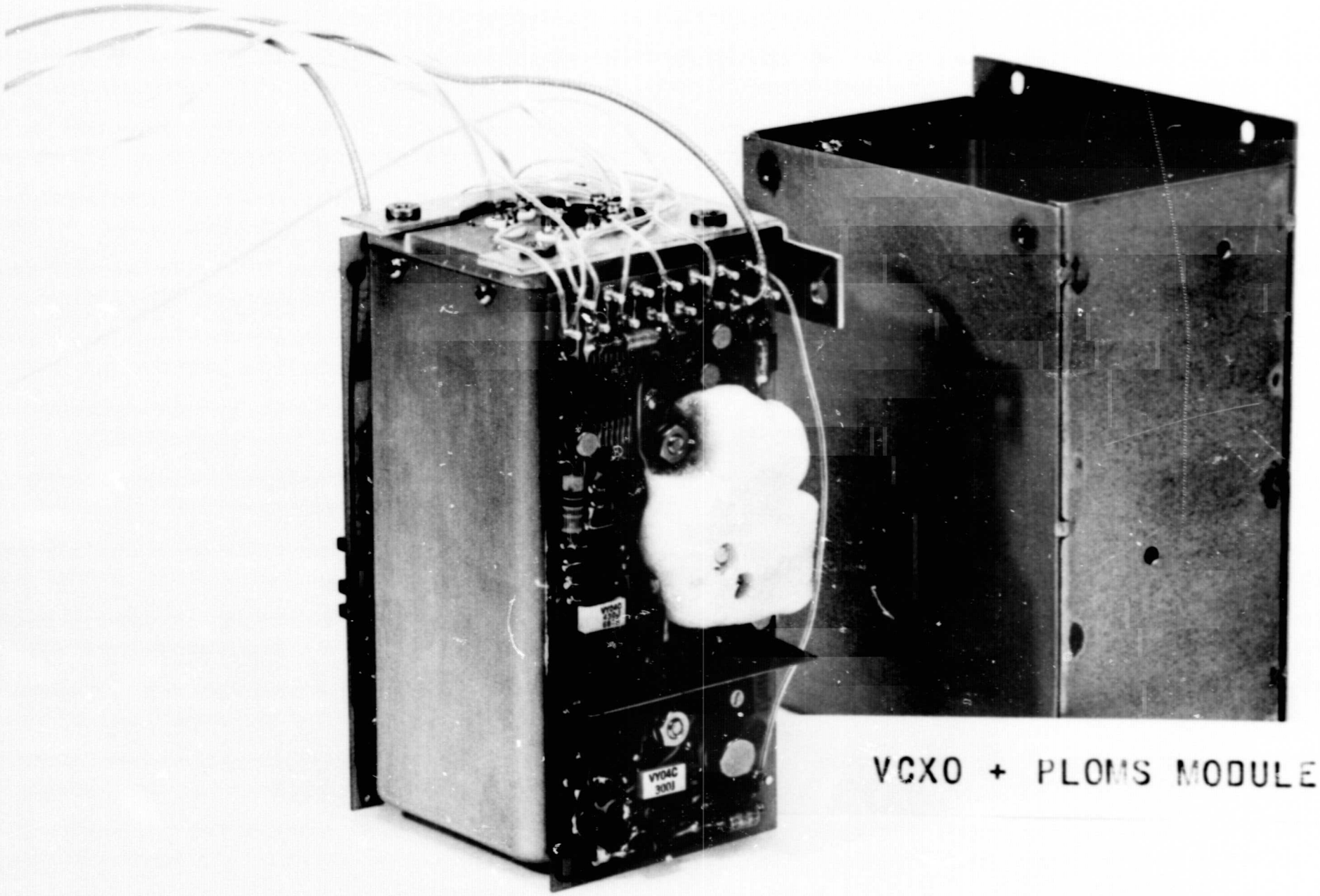
VCXO & PLOMS ASM

FIND NO.	DESCRIPTION	GR CO PART NO.	MFG PART NO	MFG CODE	NO REQ
1	VCXO BOX ASM	2995-2849			1
2	8.192 MHz OSC	2995-2850			1
3	61.44 MHz PLOM ASM	2995-4880			1
4	4.848 MHz PLOM ASM	2995-4881			1
5	NUT, HEX, .138-32 THD	1810-2400			4
6	WASHER, LOCK, SPLIT, .138	5040-1800			4
7	8.192 MHz BUFFER AMPL				1
C1,2,3	CAPACITOR, DISC	4800-8900			3
C4	CAPACITOR ARRAY 330pF		CX05		1
R30,31,32	RESISTOR, 100 Ω	12W	6100-1135		3
R7	RESISTOR 100Ω	1/4W	6099-1155		1
R3	RESISTOR 330Ω	1/8W	6098-		1
R5,6	RESISTOR 1K Ω	1/8W	6098-		2
R1	RESISTOR 33K Ω	1/8W	6099-2265		1
R2	RESISTOR 10K Ω	1/8W	6098-		1
R4	RESISTOR 1K Ω	1/8W	6098-		1
R8	RESISTOR 150Ω	1/8W	6098		1
Q1,2	TRANSISTOR			04713	2
T1	TRANSFORMER, PLOMICS	1158-0430		24355(3170)	1

NOTES:
1. APPLY PRIMER INSIDE & FILL WITH DOW CORNING SYLGARD 188. AFTER ALL CONNECTIONS ARE MADE, FILL ADDITIONAL .688 PORTION. TEMPORARILY CAULK AT BOTTOM WHERE NECESSARY. PLUG ADJUSTMENT HOLE "D" TO ALLOW ACCESS TO ADJUSTMENT HOLE "C"

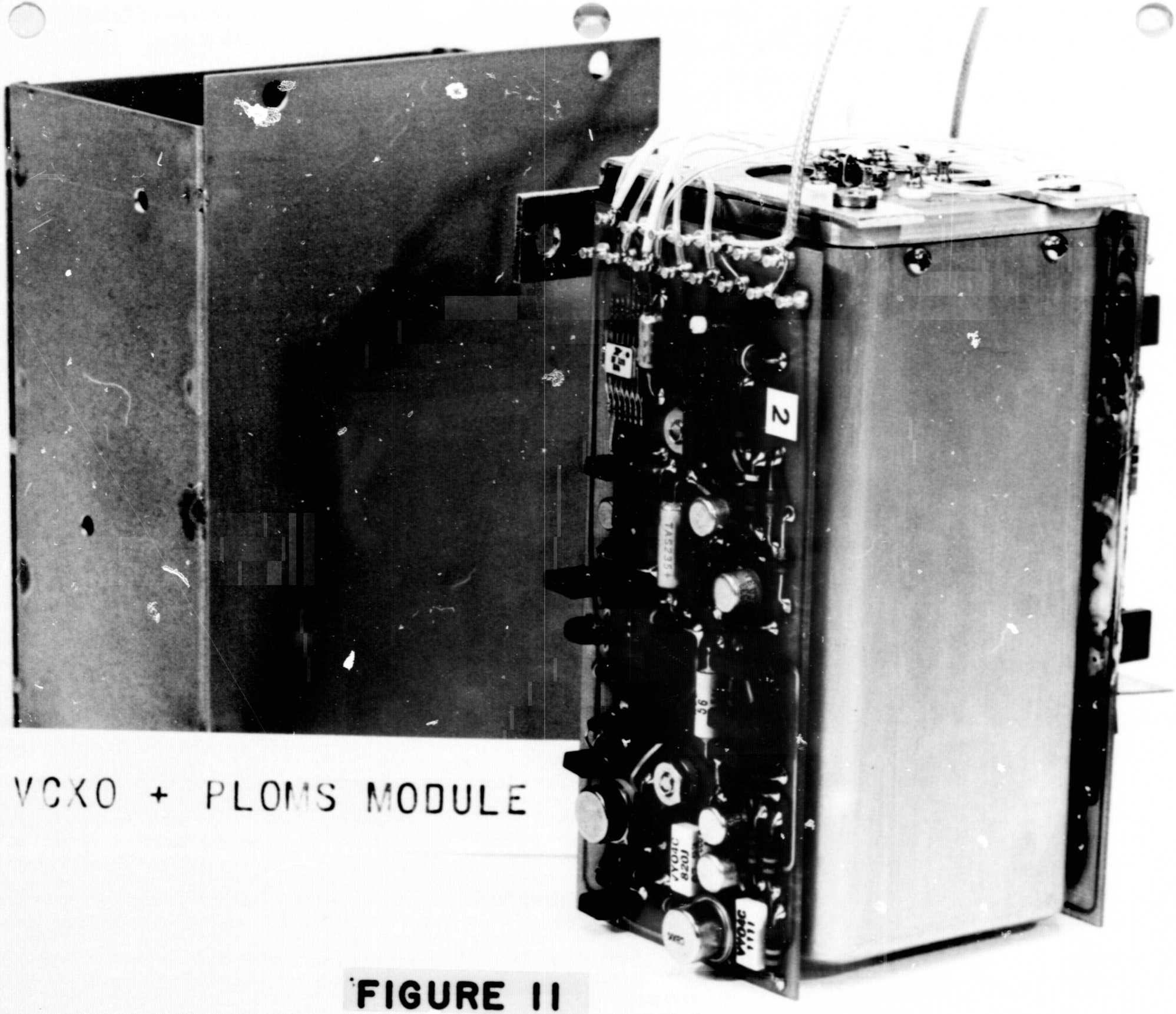
UNLESS SPECIFIED MAKE THE FOLLOWING CONNECTIONS USING ESMM-32-38-1 SERIES ENDS 16

SIGNAL	8 MHz OSC	16 MHz PLOM	61 MHz PLOM	8 MHz BUFFER	REMARKS
+V REG	WT-1				
	WT-2				
GROUND	WT-3		WT-14		
8.192 MHz	WT-4		WT-1		
VARACTOR	WT-5				
+20V	WT-6	WT-3	WT-7		
DC GROUND	WT-7	WT-10			
2048 KHz IN		WT-2	WT-5		
+5V		WT-1	WT-2		
MODULATION			WT-8		BR. COND (ESMM-BC)
MOD. GND.			WT-13		BR. SHIELD
R.F. IN			WT-10		BR. COND (ESMM-BC)
RF GND			WT-17		BR. SHIELD
N1 (IF)		WT-8			BR. COND (ESMM-BC)
40		WT-5			BR. SHIELD
	WT-6	WT-1			R30,31 & 32 IN SERIES
+20V		WT-3		WT-1	10Ω
N1				WT-2	BR. COND (ESMM-BC)
40				WT-3	BR. SHIELD
8.192 MHz	WT-4			WT-4	47Ω
SHIELD	WT-3			WT-5	



VCXO + PLOMS MODULE

FIGURE 10



VCXO + PLOMS MODULE

FIGURE 11

2.3 RF AMPLIFIER MODULE (2995-4849)

Introduction:

The 61.44 MHz RF Amplifier Module serves to amplify the -10 dBm output of the 61.44 MHz PLOM, providing a stabilized drive level of +13 dBm to the X111 Microwave Multiplier.

Block Diagram Description (See Print 2995-4849-2DA)

The 61.44 MHz RF Amplifier contains two stages, the first a cascode configuration with voltage variable gain and the second, a grounded base stage. Both are tuned to 61.44 MHz with transformer coupled outputs. The output level of the second stage is sensed by an automatic level control circuit which controls the gain of the first stage as required to maintain constant output.

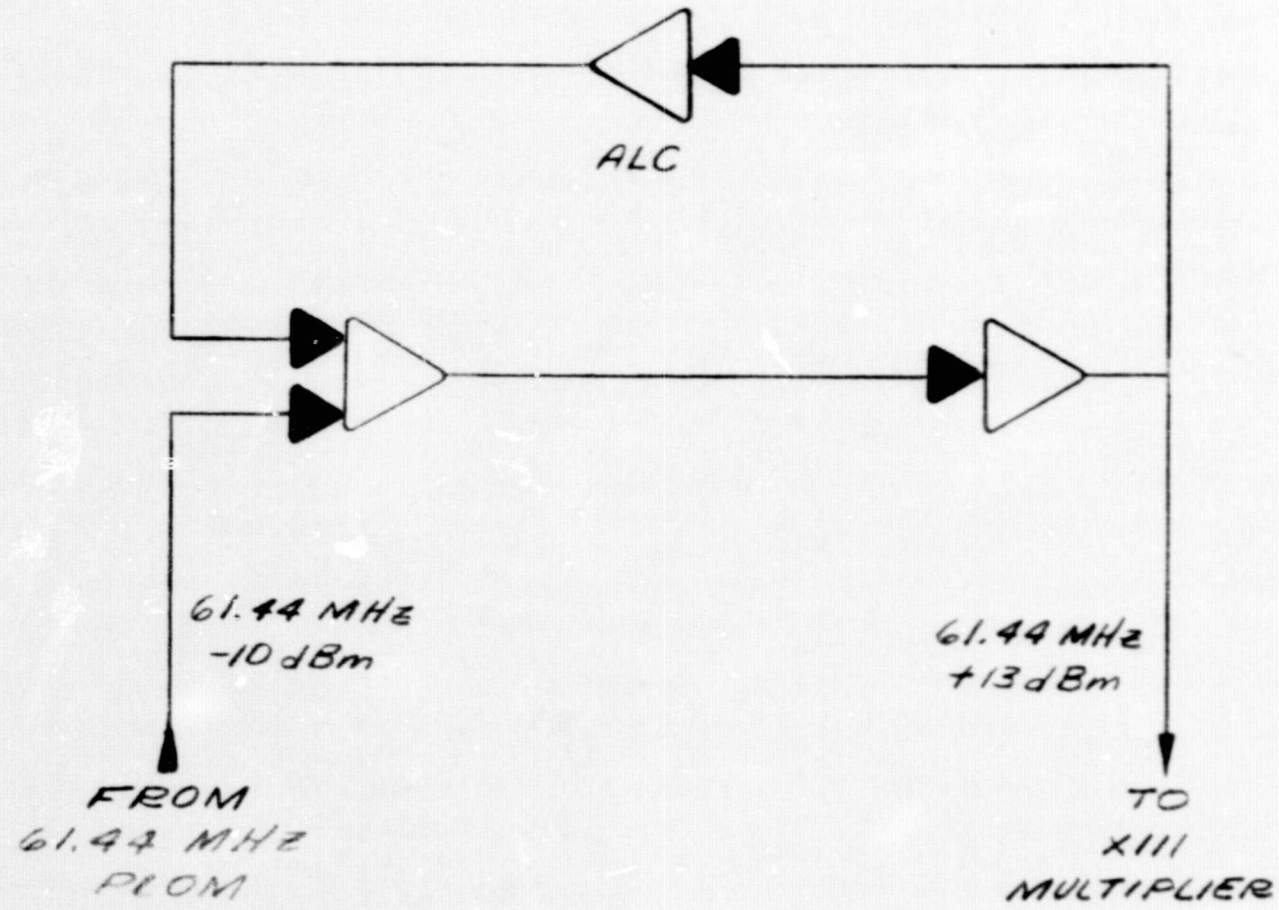
Circuit Description (See Print 2995-4849-2D)

The first stage uses an integrated circuit, IC1 consisting of a differential amplifier and active current source, connected as a cascode amplifier. The input is applied to the lower base and the output is taken from the secondary of transformer T1 whose primary resonates with C2 at 61.44 MHz. The gain of this stage is controlled by the dc voltage applied to terminals 5 and 7 which varies the dc operating current.

The second stage employs Q1 as a conventional grounded-base tuned amplifier. The output from the secondary of T2 drives the X111 Microwave Multiplier through the R6, R7, R8 attenuator network

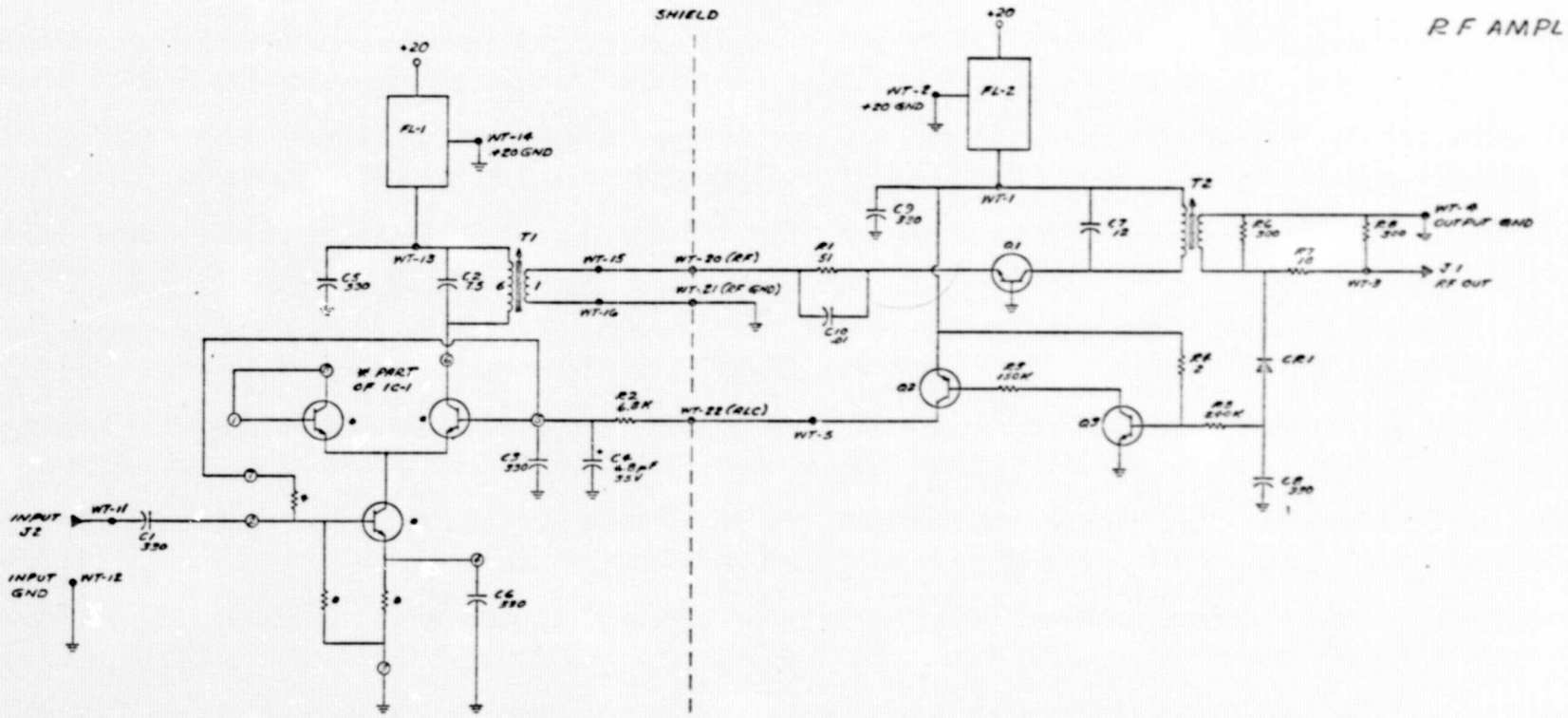
Diode CR1 operates as a negative peak detector to sense the output level at the secondary of T2. Transistors Q2 and Q3 form a dc amplifier for automatic level control.

A photo of the RF Amplifier is shown as Figure 12.



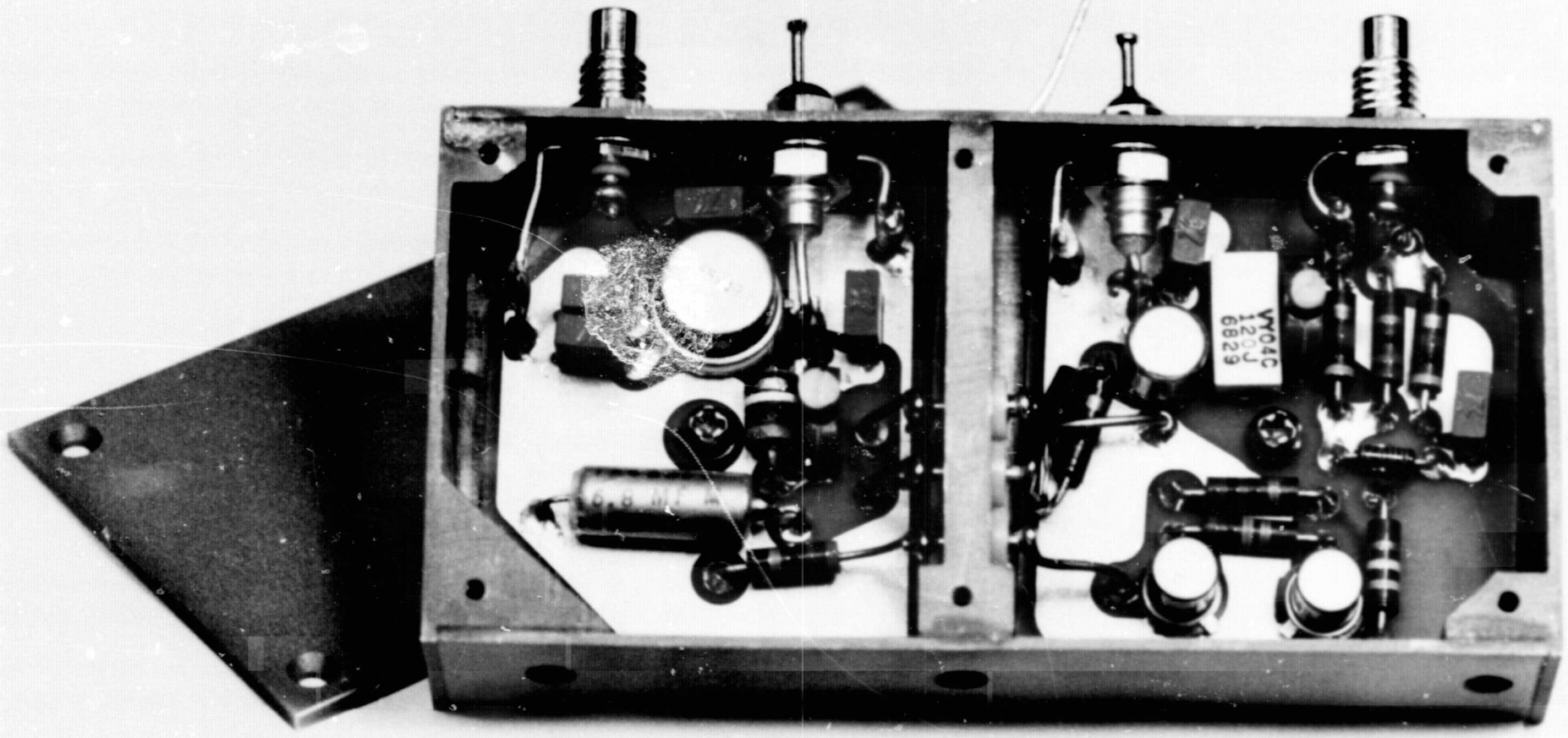
2995-4849-2DA/1
RF AMPLIFIER

R F AMPLIFIER



R F BD (#1) 2995-4884

R F BD (#2) 2995-4885



RF AMPLIFIER MODULE

FIGURE 12

2.4 MICROWAVE MULTIPLIER-MIXER MODULE (2995-4841)

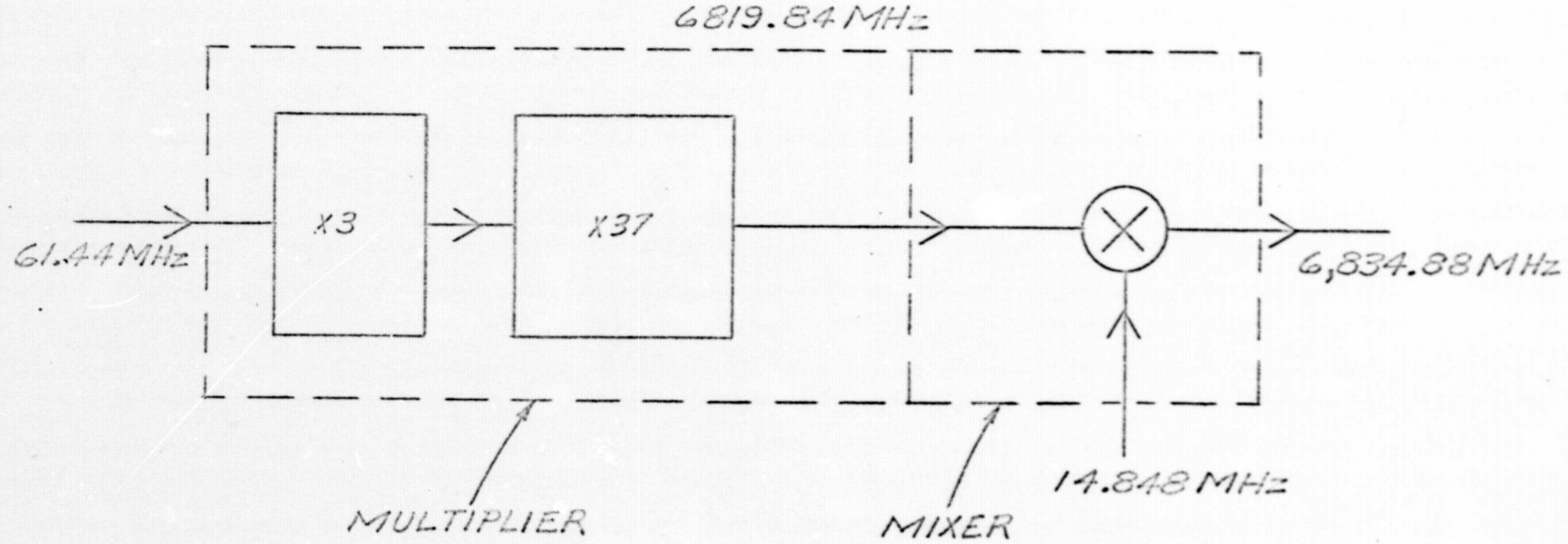
The microwave cavity within the Optical Package requires 10-30 μW of microwave power at 6,834.638 MHz for optimum excitation. This signal is obtained by multiplication of the 61.44 MHz from a phase-locked oscillator multiplier "PLOM" to 6,819.84 MHz, then mixing with 14.848 MHz. The upper sideband gives the desired signal.

Development work and production of a breadboard model and two deliverable microwave multiplier-mixers was subcontracted to Resdel Engineering Corporation, Arcadia, California. This subcontractor was selected after a careful survey of all known possible sources on the device. The final mixer was obtained from Aertech, Sunnyvale, California. Several design iterations were required.

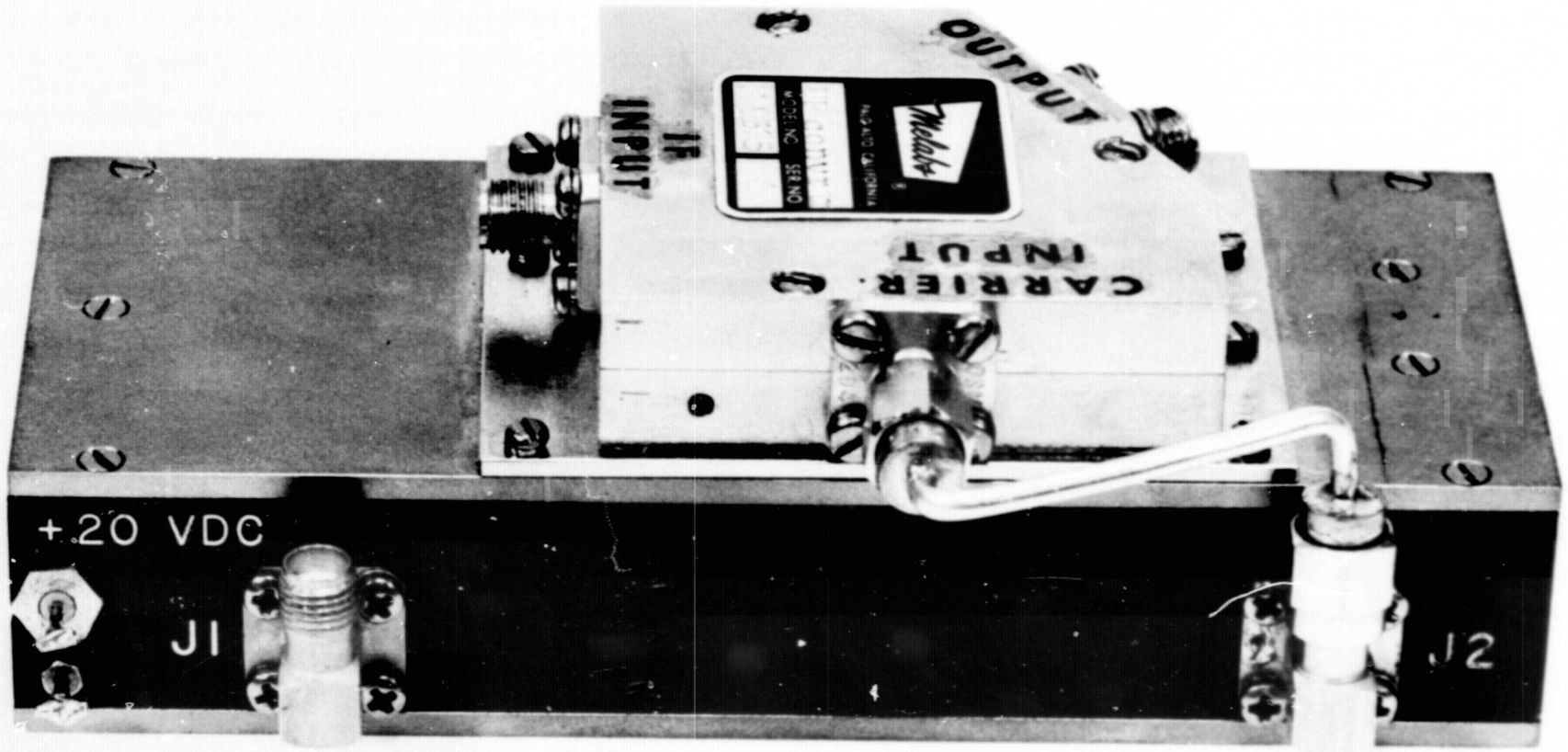
Figure 13 shows an elementary block diagram of the microwave multiplier-mixer assembly. The X111 multiplier is obtained by first multiplying by X3 with conventional tuned circuits, amplifying, then driving a step recovery diode multiplier for X37. The output power at 6,819.84 MHz is 1 mW. A balanced mixer is used to give the final output frequency and suppress the carrier signal by more than 10 dB. The mixer is Aertech Model No. MX8036.

Details of the multiplier are on Resdel Engineering drawing No. 21047B. Some design and construction details are proprietary to Resdel Engineering.

A photo of this module (using an earlier mixer section) is depicted as Figure 14.



MICROWAVE MULTIPLIER MIXER
FIG. 13



MULTIPLIER MODULE

FIGURE 14

2.5 SERVO AMPLIFIER MODULE 2995-4846

Introduction

The primary function of the Servo Amplifier is to lock the frequency of the 8.192 MHz crystal oscillator with respect to the rubidium resonance at 6834.688 MHz. This is accomplished by synchronous detector circuits which process the photodetector signal from the optical package to produce a frequency control voltage for the Master Crystal Oscillator.

A secondary function of the Servo Amplifier is to provide an indication of the lock-loop condition and, if the system is not locked, to achieve lock.

The Servo Amplifier also contains circuits for generating the frequency modulation signal that is applied to the r-f which excites the rubidium hyperfine transitions and a circuit for starting the rubidium lamp.

Block Diagram Description:

The photodetector signal from the optical package is processed as shown in print 2995-4846/2DA to accomplish these servo amplifier functions.

The photodetector signal is applied to a cascade arrangement of two synchronous detectors, the first operating at the second harmonic of the modulation rate and the second at the fundamental rate. The synchronous detectors compare the phase of their input signals with that of a reference signal from a flip-flop, producing a dc output voltage which is proportional to the amplitude of the particular signal component and the cosine of the phase difference.

The second harmonic synchronous detector therefore produces a dc voltage proportional to second harmonic signal amplitude. This voltage is applied to a threshold circuit which serves to indicate a locked condition by detecting the presence of second harmonic signal.

The fundamental synchronous detector similarly produces a dc voltage dependent on the fundamental signal component. Since the phase of this component is 180° different if the r-f excitation is above or below the center of the

rubidium resonance the output of this synchronous detector also reverses. The phasing of the overall loop is such that the integrator output changes in the direction required to bring the oscillator to the center of the line, and thus null the fundamental component. A finite amount of fundamental signal (and therefore an offset from the center of the line) is necessary to produce the voltage required to correct the crystal oscillator frequency. The dc gain of the loop however is extremely high (10^6) thus reducing a large oscillator frequency error (1×10^{-6}) to negligible proportions (1×10^{-12}). It is the function of the integrator to provide most of this high dc gain while shaping the frequency response of the loop as required for performance and stability. An additional passive frequency response shaping network follows the integrator.

The modulation rate generator and two flip-flops provide the required reference signals for the two synchronous detectors. A passive RC integrator following the fundamental flip-flop provides the triangular phase modulation signal required to produce square-wave FM in the 61.44 MHz PLOM.

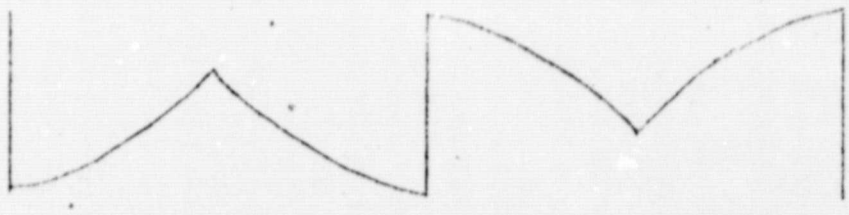
Figures 15 and 16 show the waveforms present in the cascade detector of the Servo Amplifier under unlocked conditions when the photodetector signal has a large fundamental component, and under locked conditions when it consists of a second harmonic component. The detector logic and various instrument operating conditions establish the phase relationships as shown.

Figure 15 shows that the fundamental signal component undergoes a 90° phase shift by passing through the second harmonic detector but its information content is otherwise unaffected. The fundamental synchronous detector converts the fundamental component into a dc control signal for the frequency lock loop. Furthermore, the fundamental component does not produce a dc output at the second harmonic detector.

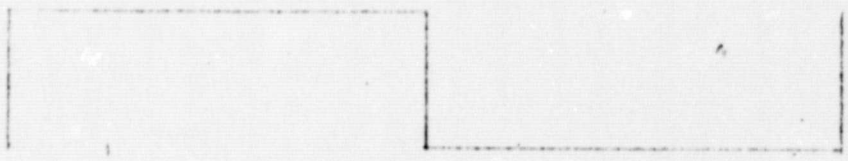
Figure 16 shows that the situation is just the reverse for a second harmonic signal component. The second harmonic detector is the one that produces a dc output while the fundamental detector does not.

FUNDAMENTAL
PHOTODETECTOR SIGNAL

2nd HARMONIC
DET SW DRIVE



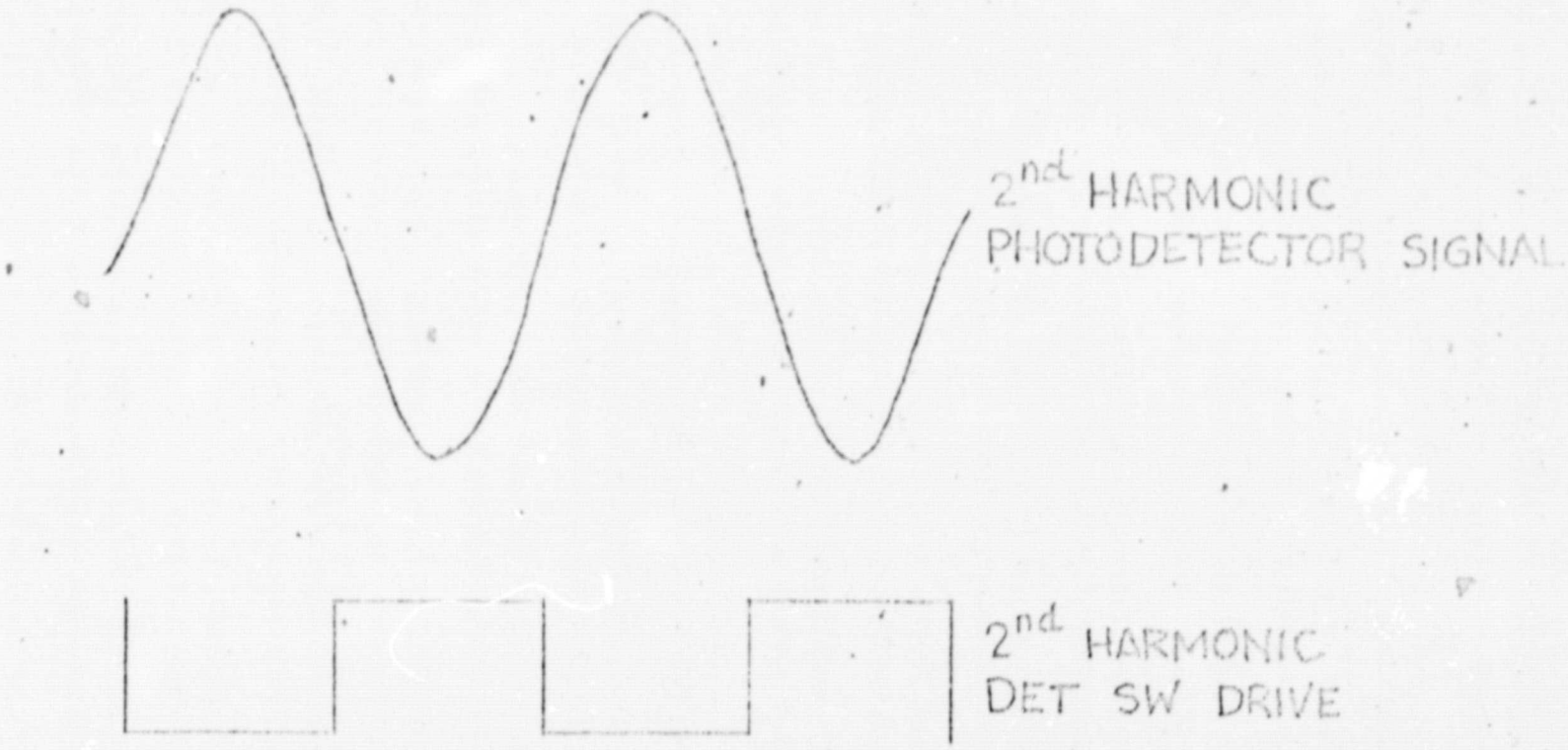
2nd HARMONIC
DET OUTPUT
(NO DC SHIFT)



FUNDAMENTAL
DET SW DRIVE

SERVO AMP WAVEFORMS
UNLOCKED CONDITION - MAX FUNDAMENTAL SIGNAL

FIG 15



LOCKED CONDITION— SERVO AMP WAVEFORMS

FIG 16

The basic operation of this cascade detector arrangement is therefore the same as would result if each detector processed the photodetector signal independently. It has the advantage of requiring less hardware and, by shifting the second harmonic signal to fourth harmonic ahead of the fundamental detector, improves the dynamic range of the servo amplifier. The fundamental component must be detected in the presence of a much larger second harmonic signal which can be more easily filtered out after conversion to a fourth harmonic rate.

The fundamental synchronous detector and integrator are the most critical elements of the servo amplifier because dc signal levels in these circuits directly affect the SATS output frequency. Any dc offset will introduce a frequency offset and, most important, a change in dc conditions will cause a frequency change. The sensitivity at this point is such that a 3 mV dc change would cause a frequency change of about 1×10^{-11}. This is the approximate effect of the servo amplifier on the SATS output frequency over the entire environmental temperature range.

Initial lock of the frequency control servo is obtained by sweeping the frequency of the 8.192 MHz crystal oscillator until the rubidium resonance is reached. This is accomplished by the search oscillator under control of the second harmonic detector signal threshold circuit. It is a squarewave generator which drives the integrator through a resistor, thus producing the desired sweep voltage for the crystal oscillator. Relay contacts provide a monitor indication of lock.

The lamp starter circuit included on the servo amplifier assembly senses the dc voltage from the photodetector preamplifier and changes the lamp oscillator bias to insure that the rubidium lamp is properly lit.

Circuit Description (See Print 2995-4846-2D)

The photodetector signal input to the servo amplifier is applied to the second harmonic detector, the lamp starter circuit and resistor R17, the light monitor output.

Zener diode CR2 serves to turn on Q2 if the dc output from the photodetector preamplifier is low about 7.3 volts. Thus, if the rubidium lamp output is low, additional dc bias current determined by R1 is applied to the lamp oscillator circuit to start the lamp and insure it is operating in a mode with sufficient light output.

The ac photodetector signal is coupled through C1 to T1 which provides bi-phase drive to the second harmonic synchronous detector switches Q1-A and Q1-B. These are p-channel enhancement mode MOS field-effect transistors which are turned on and off for alternate half-cycles at the second harmonic rate by the second-harmonic flip-flop, one section of IC3. This configuration forms a full-wave synchronous detector driving amplifier IC1 with a gain established by the ratio of R6 to R1 (or R2). Capacitor C2 introduces high-frequency rolloff with a break at about the fourth-harmonic frequency. A dc reference level of +13 V is provided by R19 and R20 and the detector phasing is such that the second-harmonic signal lowers the output voltage of IC1 as the signal increases. Resistor R8 drives the signal monitor output while R9 goes to the signal threshold detector.

Zener diode CR1 and transistor Q5 form this threshold circuit which drives Q6 and holds its collector at +20 V unless a signal is present sufficient to drop the voltage at the second-harmonic detector below about 11 volts. The switched +20 V buss at the collector of Q6 drives relay K1 (unlock alarm contacts), the search oscillator, and relay K2 which applies the search oscillator signal to the servo integrator.

The search oscillator is a relaxation oscillator using two 4-layer diodes Q7 and Q8 and is timed by R13, R14, C6 and C7. It drives Q10, producing a square-wave voltage at the junction of R15 and R16 which swings symmetrically above and below the +13-volt reference voltage.

After being processed by the second-harmonic detector the photodetector signal is coupled through C4 to T2 which provides bi-phase drive for the fundamental detector. It is identical in operation, except that it is driven at the

fundamental rate and the amplifier IC2 is used as an integrator with a time constant determined by R10 (or R11) and C6.

This detector and amplifier are the most critical elements which determine servo amplifier performance. The MOS FET type is chosen to have low leakage current. The amplifier must have low input bias current, low offset voltage and offset voltage temperature coefficient.

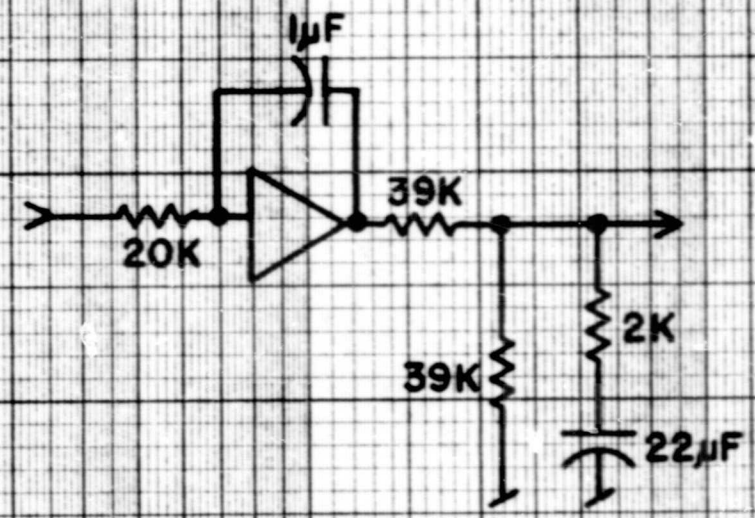
The circuit elements R16, R17, R18 and C9 provide shaping of the loop frequency response as required for stability. Figure 17 shows the Servo frequency response.

The search oscillator signal is applied to the integrator through R23, R22 drives the lock voltage monitor output.

Unijunction transistor Q3 is used as a relaxation oscillator to generate a fourth harmonic rate pulse train which drives the 2nd harmonic reference flip-flop through Q4. The R21, C12 network forms a passive integrator which produces a triangular wave fundamental modulation signal coupled through C13 to the 61.44 MHz PLOM.

Figures 18 and 19 are photographs of the Servo Module.

FIGURE 17
SERVO LOOP FREQUENCY RESPONSE

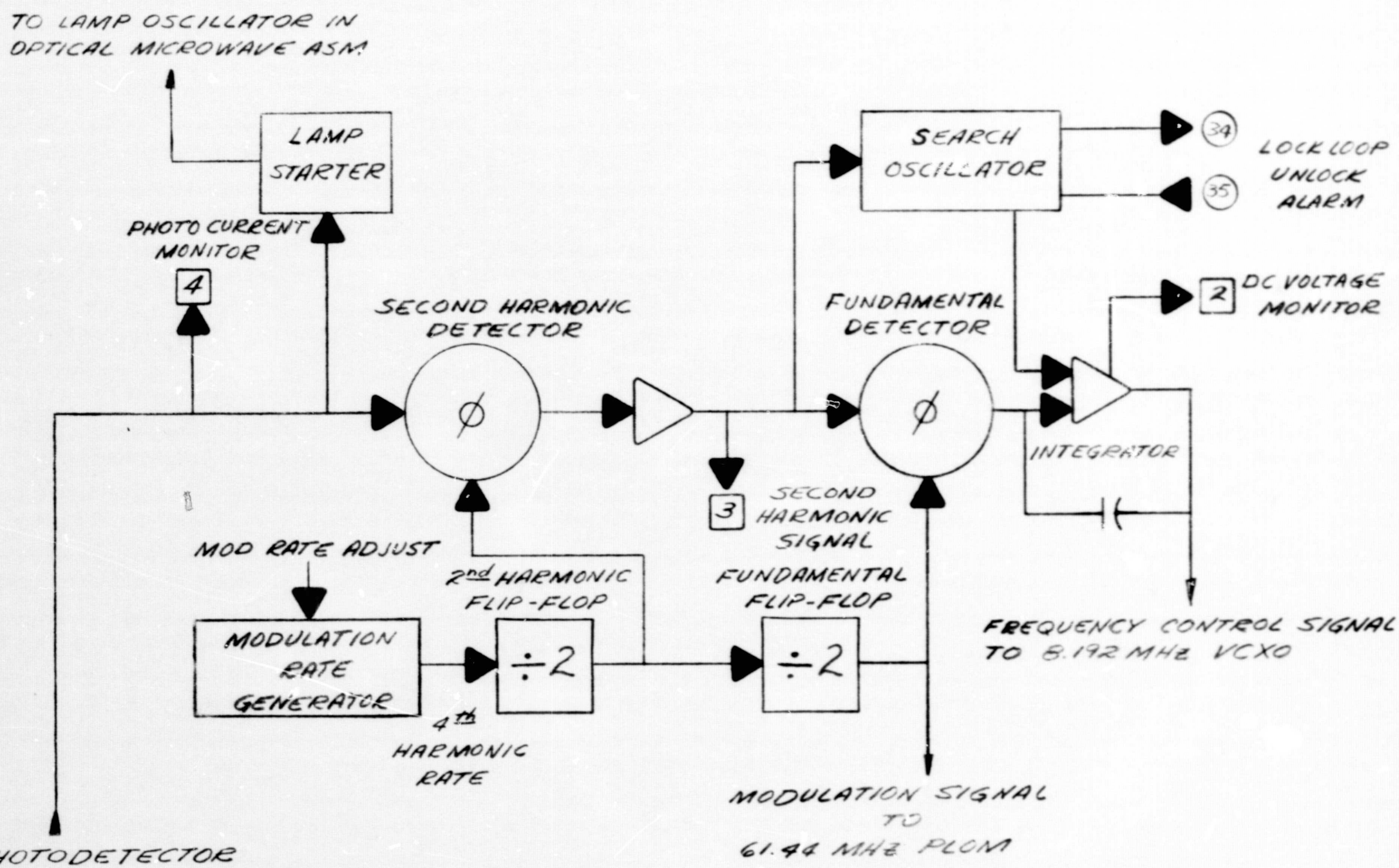


100
80
60
40
20
0

LOOP GAIN, dB

0.01
0.1
1
10
100

FREQUENCY, Hz



2995-4846-2DA/1

SERVO AMPLIFIER

SYMBOL	DESIGNATION	DWG REF
□	MONITOR PLUG (PL-2)	2995-9159-10
○	BURNERD SOCKET (SO-11)	2995-3840
△	POWER SUPPLY	2995-3840
○	VCXO & PLOMB	2995-3840

SERVO BD(#1) 2995-4871

PHOTO SIGNAL IN

(DC GND) WT-16

WT-3 C1 100μF T1 R1 10K 1W Q1-A R2 10K 1W Q1-B

R5 10K 1W IC1 R6 332K 1W C2 220pF C5 30pF C4 100μF T2 R10 20K 1W Q2A R11 20K 1W Q2-B

R8 330K R4 330K R16 330K R13 330K R12 150K R9 10K IC3 R21 100K C12 0.1μF C13 1μF

R20 2K C10 10μF

R25 200K C11 6.8μF (SEARCH OSC IN) C6 1μF IC2 C7 30pF R19 1K R24 23K R17 39K C9 22μF R18 2K R22 390K +12V

WT-10 WT-18 WT-20 WT-13 WT-11 WT-6 WT-24 WT-14 WT-12 WT-9 WT-4

MM → 1 61 MIN. FLOW (+20V)

PP → 5 VCXO (VARACTOR CONTROL) 6

RR → 2 INTEGRATOR METER

RR → 3 61 MIN. FLOW (MOD SIG.) 4

(MOD RATE IN) WT-8 WT-25 WT-1

END HARMONIC METER 9

(END HARMONIC DC OUT)

SERVO BD (#2) 2995-4872

LIGHT METER 4

WT-23 R17 330K R2 470 R3 1K Q2 CR2 (-12V) C1 15μF 20V R1 10K C2 .0047μF R7 51 C3 .001μF R8 10K Q3 Q4 R6 375K CR1 R5 10K R6 220 R9 10K C8 4.8μF

WT-3 WT-21 (PHOTO SIG IN)

LAMP START OUT 10

MM WT-12 WT-16 (DC GND) WT-24

WT-8 WT-26 (MOD. RATE OUT)

R10 47K Q6 R11 2K Q5 C5 4.8μF CR1 C4 47μF

K2-1 K1 R13 27K C6 100μF Q7 R14 27K C7 100μF Q8 K2-2 R15 27K R16 2K Q10 CR3

(+30V) WT-27 WT-10

WT-22 UNLOCK LIGHT CONTACT #1

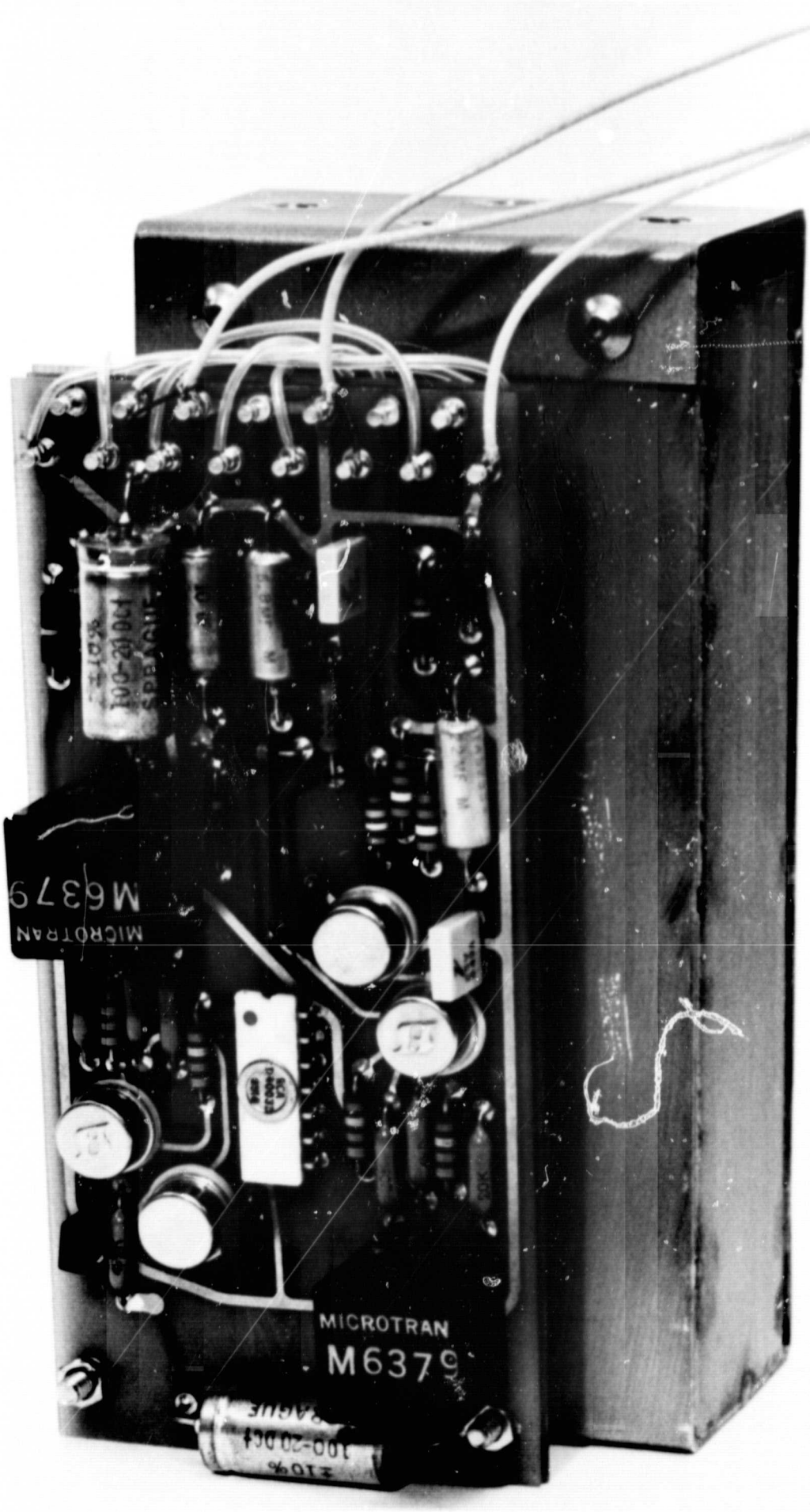
SEARCH OSC OUT WT-14 WT-20

WT-22 UNLOCK LIGHT CONTACT #2

(END HARMONIC DC IN) WT-39 WT-4

(+12V) WT-24 WT-6

* VALUE DETERMINED IN TEST



SERVO MODULE

FIGURE 18

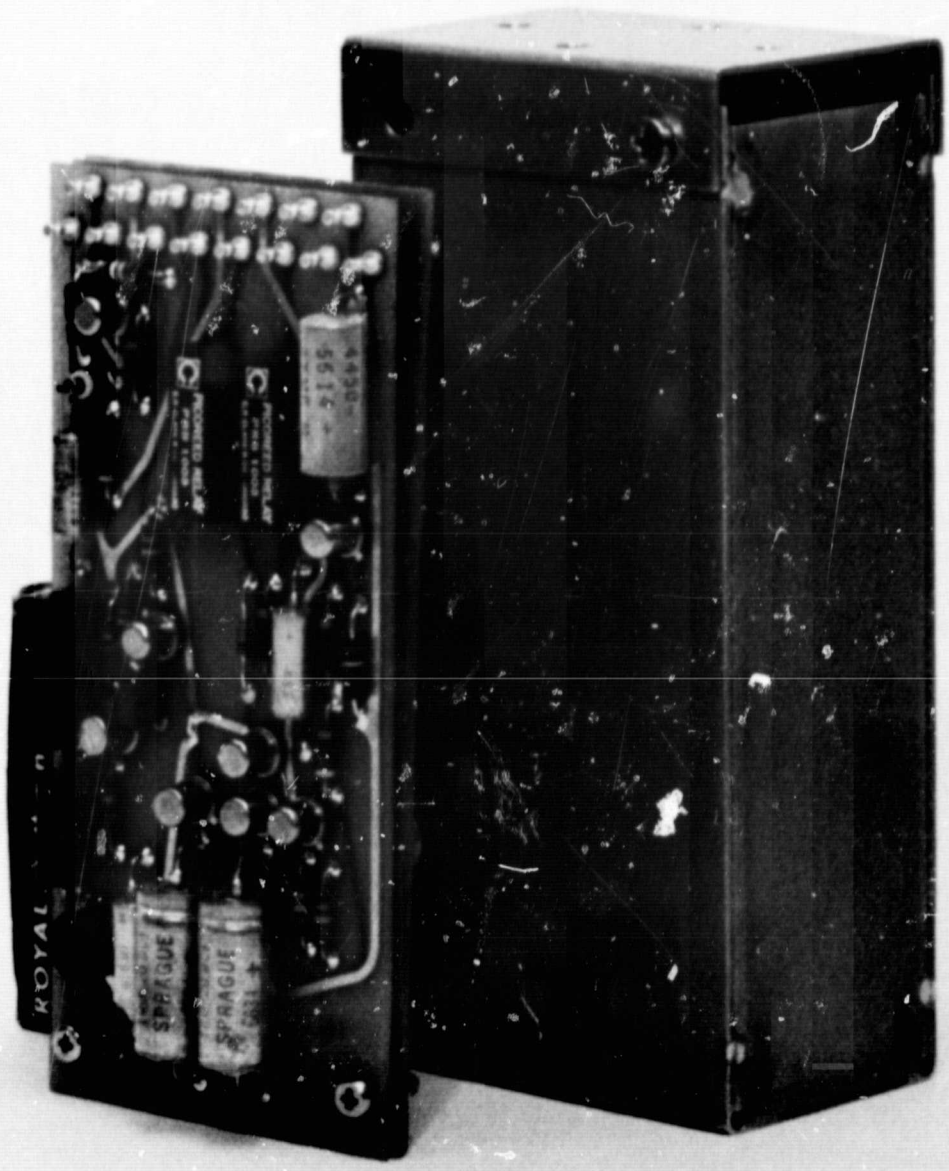


FIGURE 19

2.6 HEATER CONTROL CIRCUITS FOR OPTICAL PACKAGE (2995-4845)

Ovens in the Optical Package are used to maintain constant temperature of three areas: lamp, microwave cavity and tip sink for cell tubulations. Controllers for these ovens are located on the heater control board. The lamp and microwave cavity controllers are switching type chosen for high power efficiency. The tip heater controller is dissipative.

Thermistors, heat-sunk to the ovens, form the sense element for the controllers. This thermistor forms one arm of a bridge. The unbalance voltage of the bridge is amplified and used to control the current to the heaters.

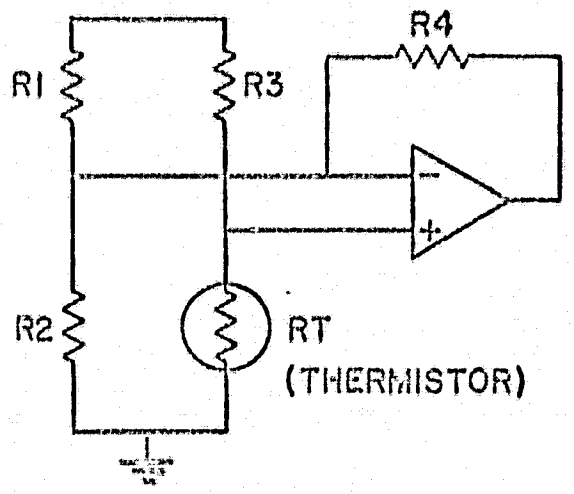


Figure 20 Bridge and Unbalance Voltage Amplifier

In Figure 20, R_1, R_2, and R_3 are precision resistors with very low temperature coefficients. The amplifier is a monolithic operational amplifier with gain near balance determined by the ratio of R_4 to the parallel combination of R_1 and R_2 (or R_3 and R_T). The maximum usable overall gain of the heater controller is determined by the thermal design of the oven. R_4 is chosen for maximum stable gain.

Tip-Heater Controller (Figure 21)

The tip heater current is controlled by Q_7 acting as a series pass transistor from the 35-V supply. The tip heater resistance is 1 kΩ, thus the maximum dissipation of Q_7 is 300 mW. The transistor is rated at 1-watt dissipation in free air at 25°C. The drive for Q_7 comes from the emitter of Q_6 through zener

diode CR_2. The zener diode provides a voltage translation to permit Q_6 to be driven from an operational amplifier operating near the center of its output voltage range. R_{20} is a holdback resistor for Q_7. The heater turns on when the voltage at the base of Q_6 exceeds $V_Z + 2\ V_{BE}$. This base voltage is determined by feedback resistor R_{39} connected to the low side of the tip heater and R_{18} coming from the operational amplifier output.

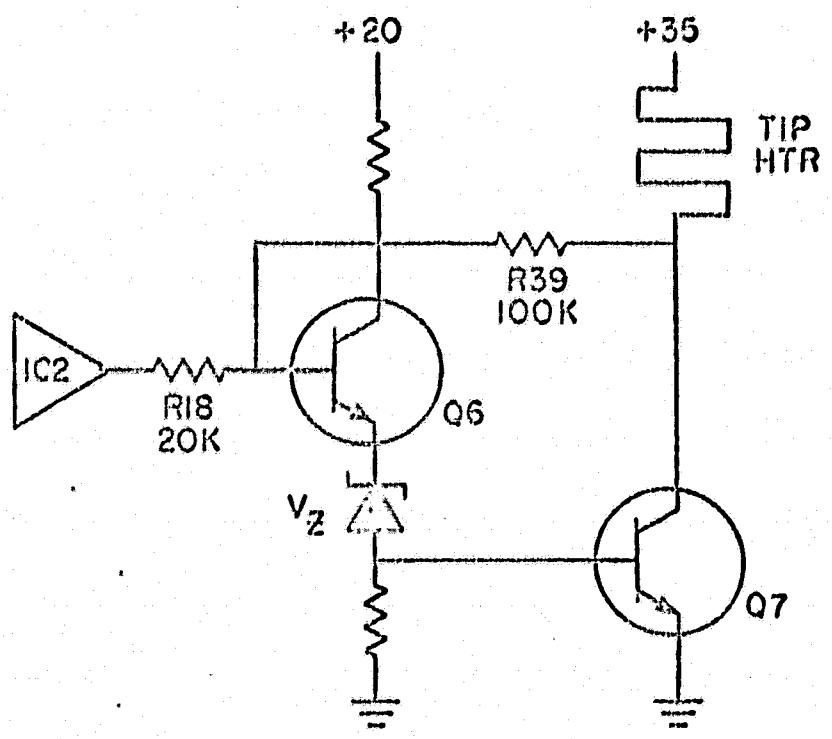


Figure 21 Tip Heater Controller

The heater turn-on threshold occurs at 6.2 V from IC2. The heater is full on when this voltage is greater than 13.2 V.

MAIN OVEN AND LAMP HEATER CONTROLLER (see Print 2995-4870-2D/2)

Both the main and lamp heater controllers are switched at a 20-kHz rate (nominal). The duty ratio varies proportionally with the required power for each oven.

The power for the main heater and the power for lamp heater after warmup are such that less than 50% duty ratio is required for each even at -34°C, the lowest environmental temperature. To reduce ripple current on the 35-V power supply the two controllers are designed to operate out of phase with one another. This phase change is accomplished in the drive to the switch.

Control of the duty ratio is done by comparing the dc output from the bridge amplifier with a 5-volt peak-to-peak, 20-kHz triangular wave, biased at +10 volts dc. The comparison is done by Q_8 and Q_9 for the main heater and Q_{12} and Q_{13} for the lamp heater.

The main heater is on when Q_9 and Q_{10} are off. This occurs when the dc voltage from the bridge amplifier is more negative than the triangular wave voltage. The main heater turns off when the triangular wave voltage becomes the more negative. The connections of the thermistor bridge to the amplifier (IC3) are reversed from those shown in Figure 20 to provide proper phasing of the controller.

The lamp heater uses the bridge-amplifier connections shown in Figure 20. Here the heater comes on when Q_{13} and Q_{14} are on. The voltage comparator is identical to that used in the main heater controller.

Some details on the circuitry that are not obvious from the schematic diagram are:

(1) Q_7, Q_{10}, and Q_{14} are power transistors rated at 6 A which are selected for low V_{CE} at lowest operating temperature.

(2) Two diodes in the comparator circuit provide reverse base emitter breakdown protection for the PNP transistors.

(3) The 6-volt power supply is used to drive Q_{10} and Q_{14} to reduce dissipation in drive circuit to switching transistors.

(4) Q_{16} provides protection against overheating in the event the 20-V power supply is shorted or disconnected. (Loss of the 6-V and/or 35-V supply will cause all heaters to shut off.)

(5) Monitors for the heaters are provided by a 240-kΩ resistor to the collector of each series transistor.

TRIANGULAR WAVE GENERATOR

The triangular wave generator supplies the ramp voltage to the comparators in the switching heater regulators. The linear operating range of the controller is determined by the range the bridge amplifier can swing between thresholds where the heater just turns on and where it is full on. This linear range is equal to the peak-to-peak voltage to which it is compared, i.e., the peak-to-peak voltage of the triangular wave. Thus the higher the peak-to-peak voltage of the triangular wave, the larger the linear range of the controller and the lower the overall gain of the controller. Thus the amplitude of the triangular wave determines the gain of the controller.

The triangular wave is generated by integrating a square wave with IC1. The peak-to-peak triangular wave amplitude is controlled by comparing with a square wave with well defined on and off levels. The differential amplifier compares $V_{triangle}$ with the voltage at the collector of Q_4. When $V_{triangle}$ is greater than the voltage at the base of Q_2, Q_1 is on, Q_2 off which holds Q_4 off. With Q_4 off the voltage at input to integrator is 14.75 V. This causes the integrator output to decrease. When it reaches the voltage now at the base of Q_2 (7.5 V), Q_2 turns on, Q_4 turns on, Q_5 turns on and the voltage to the input to the integrator jumps to 4.75 V. This now causes the integrator output to increase. This will increase until it reaches the new voltage at the base of Q_2 (12.5 V). At this time Q_1 turns on, Q_2 off, Q_4 off, Q_5 off and voltage into integrator is again 14.75 V.

Thus the triangular wave voltage can vary between 7.5 V and 12.5 V dc as determined by the two possible states for the voltage at the base of Q_2.

The period is determined by the gain of the integrator, $\frac{1}{RC}$ (50,000), the peak-to-peak output voltage swing and the difference between the 9-volt reference and the amplitude of the square wave being integrated.

$$T = 2 \frac{E_{OUT}}{(1/RC)E_{in}} = 50 \text{ ms}$$

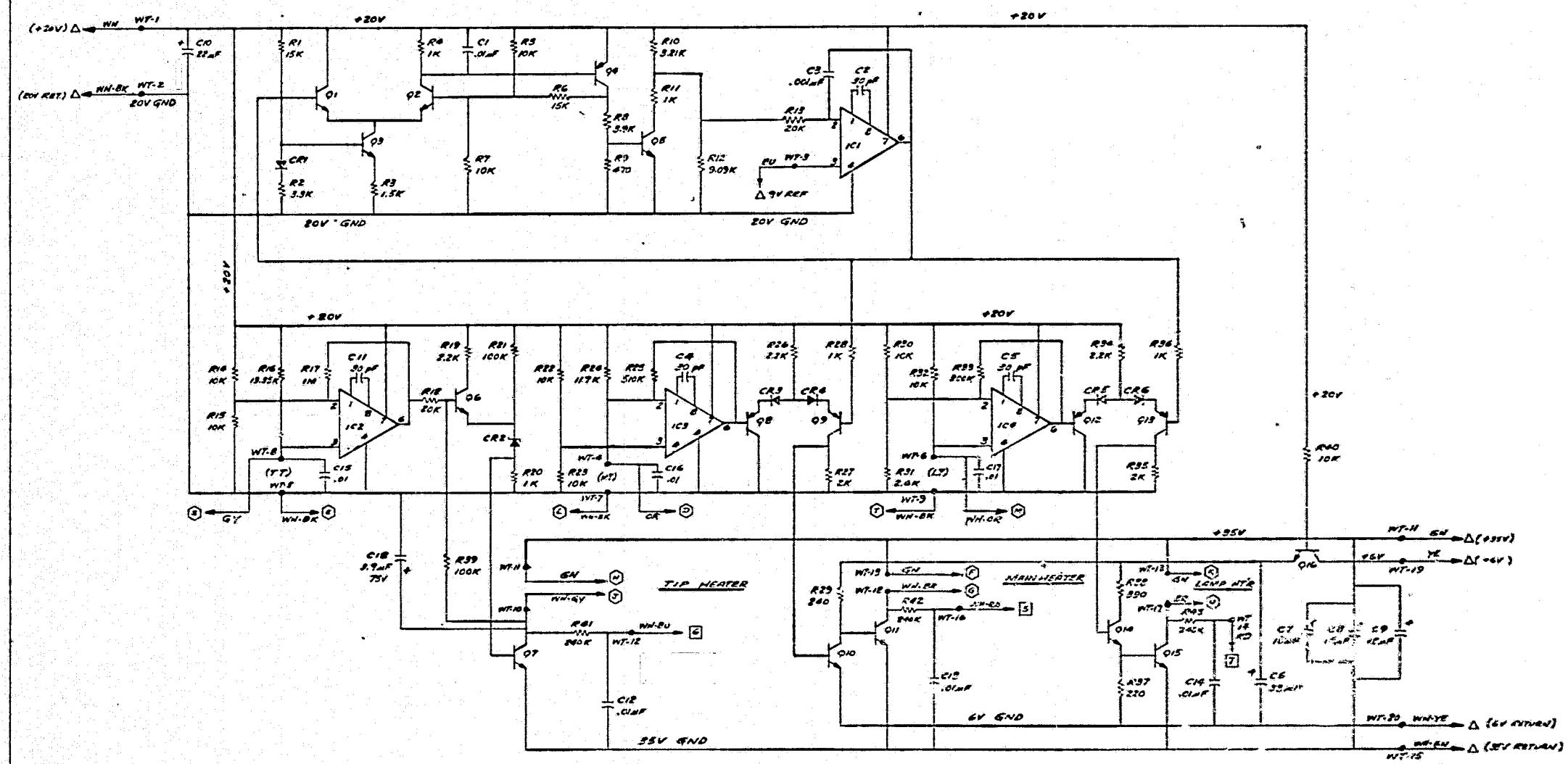
Variations in the period do not affect the temperature in the ovens, only the switching rate.

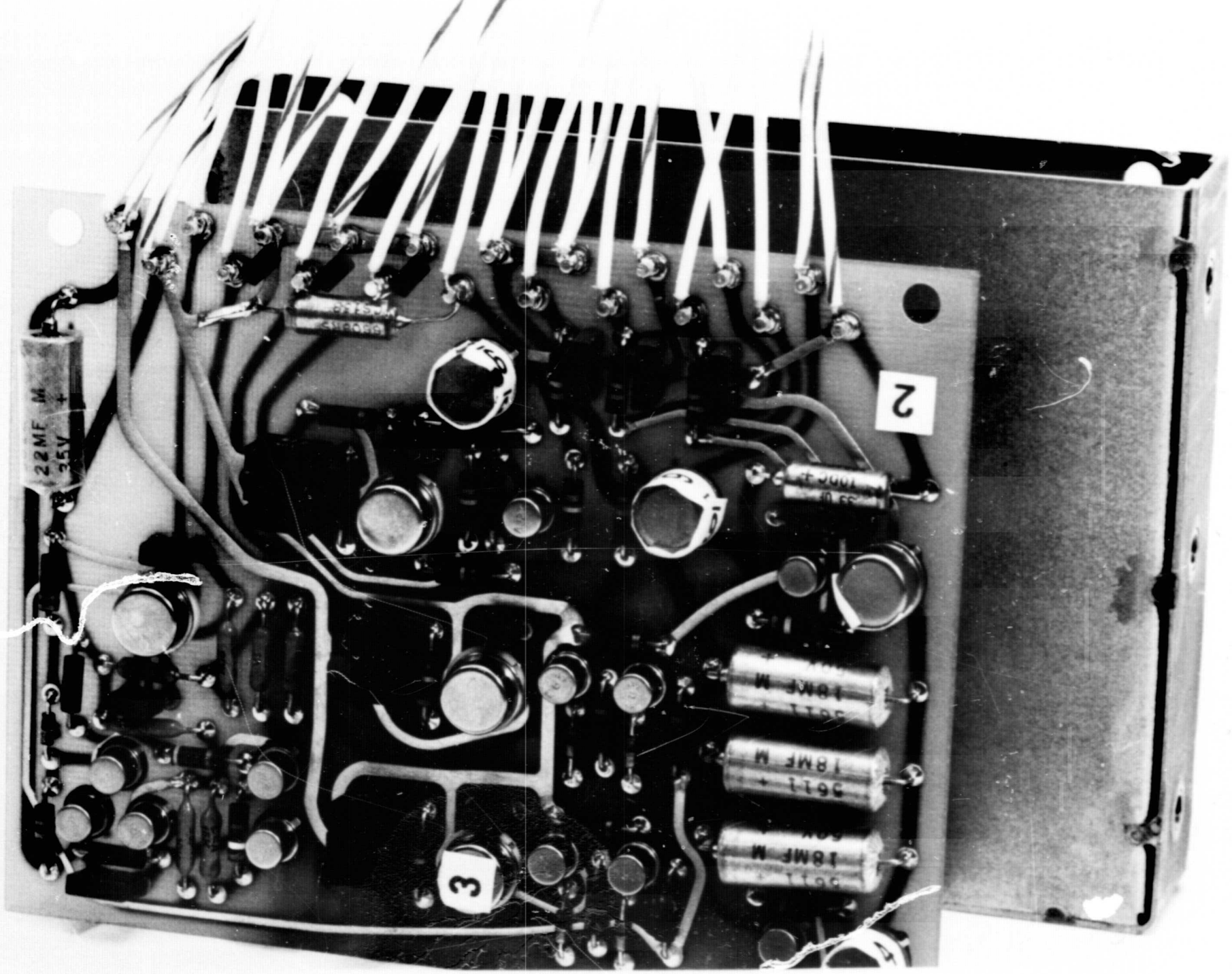
A photograph of the Heater Control Module is shown as Figure 22.

SYMBOL	DESIGNATION	DWG. REF.
□	MONITOR PLUG (PL-1)	2995-9159-10
○	BULKHEAD SOCKET (J0-1)	2995-3840
△	POWER SUPPLY	2995-3840

REVISIONS			
NO.	DESCRIPTION	DATE	APPROVED
1			
2			

HEATER CONTROLLERS CIRCUIT





HEATER CONTROLLER MODULE

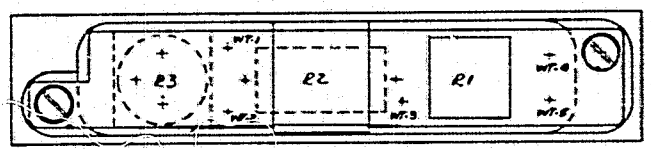
FIGURE 22

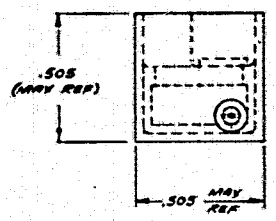
2.7 Magnetic Bias Module (2995-4850)

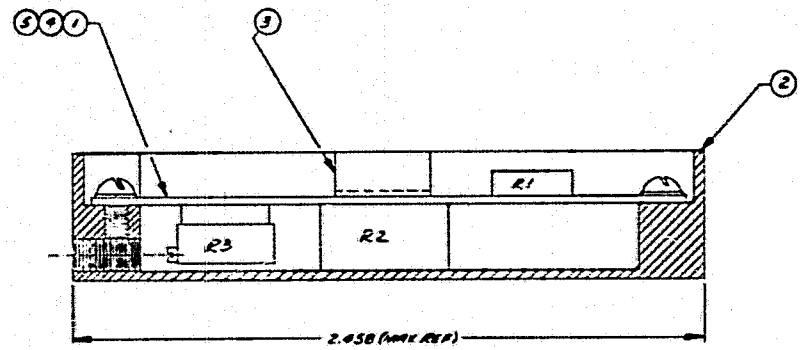
Fine frequency adjustment is accomplished by varying the magnetic field surrounding the microwave cavity. The frequency shift with magnetic field is +574 H^2 hertz at the microwave frequency where H is the strength magnetic field in gauss. The field bias is obtained from the regulated 20 V power supply using the circuit shown in print 2995-4850/2.Coarse adjustment is made by selecting R_1 which sets the frequency at low end of the adjustment range. Adjusting R_3 performs the fine frequency adjustment. This is a 20-turn potentiometer accessible by a screwdriver through a hole in the SATS side cover.

Total frequency adjustment range is approximately 1×10^{-9}. The use of R_3 as a potentiometer rather than as series resistor to the 20-V supply provides first-order temperature compensation for changes of resistance of R_3. Both R_1 and R_2 are very low temperature coefficient resistors.

FIND NO	DESCRIPTION	GR CO PART NO	MFG PART NO	MFG CODE	NO PER
1	MAG AMP BOARD	2995-5863		24655	1
2	CASE	2995-2844		24655	1
3	SHAPED RETAINER	2995-2842		24655	1
4	SCREW (SOCKET, 125)	9-90-6002			4
5	WASHER #56	2003-2008			4
6					



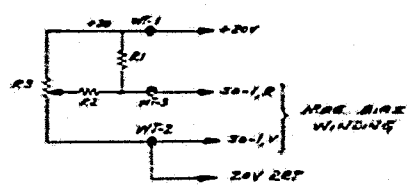




MAG-BIAS NETWORK

MAKE THE FOLLOWING CONNECTIONS USING ESMM-33-18-1

WT-1	TO	+28V	SEE DWG 2995-2844
WT-2	TO	30-1, V	
WT-3	TO	30-1, R	
WT-4	TO	20V RET	



2.8 POWER SUPPLY (2995-4840)

The power supply for the SATS converts the input supply voltage of 22 to 34 volts dc to four outputs for electronic circuits and heaters. The output voltages and their uses are:

(1) +5.4 V: Digital circuits of clock; some output buffers.

(2) +6.0 V: Output buffers and drive to heater-switching transistors.

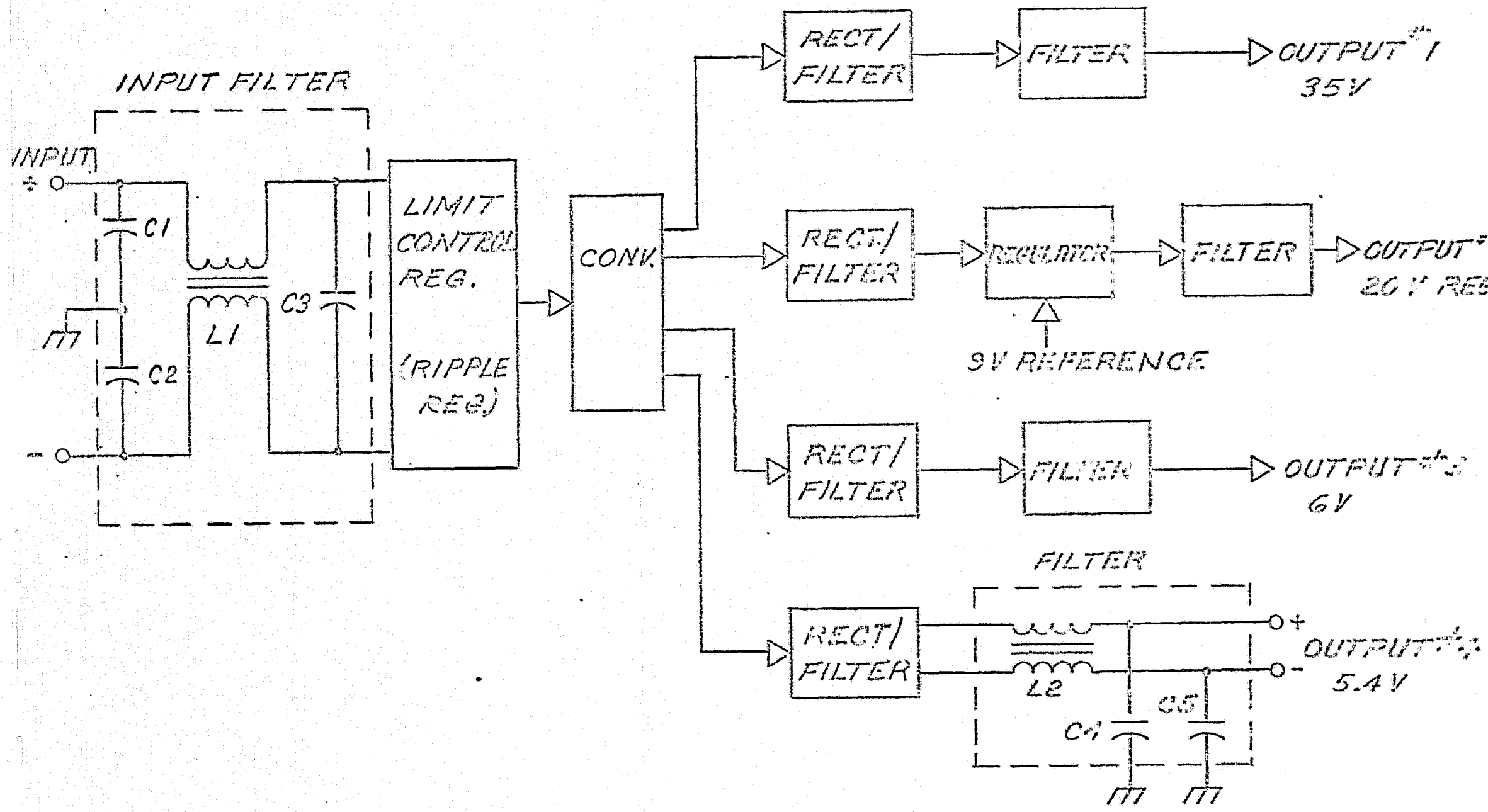
(3) +20 V Regulated: All other electronics and heater for Master Crystal Oscillator.

(4) +35 V: Heaters for Optical Package.

Complete specifications for the Power Supply are in Print 2995-4840-1/1. The power supply breadboard development and the deliverable production units were subcontracted to Gulton Industries, Inc., Hawthorne, California.

Figure 23 shows the block diagram of the power supply. The input is preceded by a series diode for reverse input voltage protection. The limit control regulator produces 19.6 V into the power converter. Rectifier and filters produce the outputs for 5.4-V, 6.0-V, and 35-V supplies. The 20-V supply contains a series regulator. The reference voltage for the regulator is a 9.0-V Zener diode located within the Master Crystal Oscillator oven. This permits excellent voltage stability over the environmental temperature range for all the electronic circuits using the 20-volt supply. Electronic short-circuit protection is provided for the 20-V and 35-V supplies. The 5.4-V and 6.0-V supplies are protected by fuses. Details of the circuit design are proprietary to Gulton Industries.

The two production units delivered by the subcontractor achieved greater than 79% efficiency at full load over the entire temperature range. The voltage change in the 20-V supply was less than 15 mV for combined effects of input voltage and temperature. Feedback ripple current is less than 60 mA under all conditions and typically less than 20 mA. Noise and ripple on the outputs were well within the desired specifications. Figure 24 is a photograph of the unit.



SAT'S POWER SUPPLY
FIG. 23

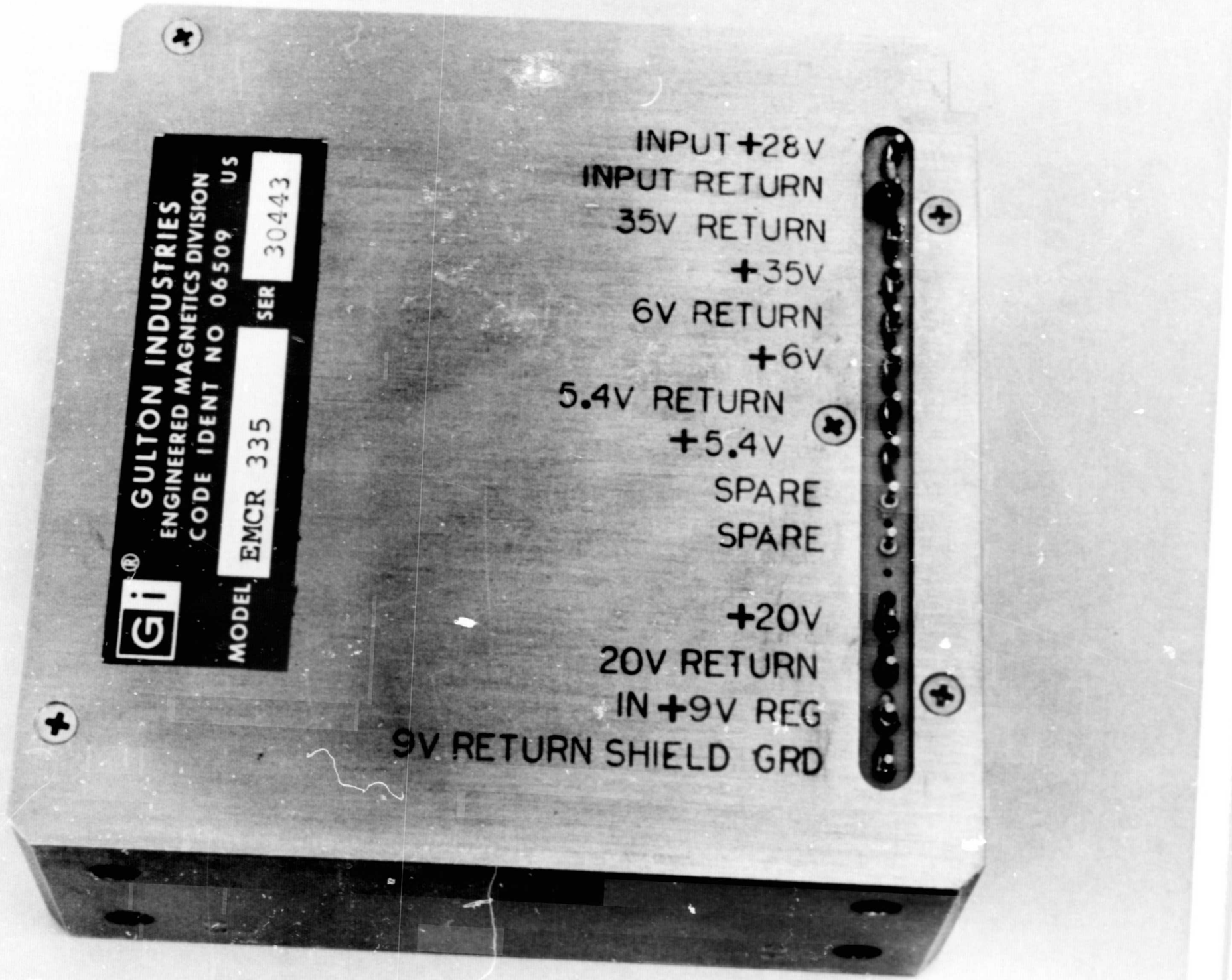

GULTON INDUSTRIES
ENGINEERED MAGNETICS DIVISION
CODE IDENT NO 06509 US
MODEL EMCR 335
SER 30443
INPUT +28V
INPUT RETURN
35V RETURN
+35V
6V RETURN
+6V
5.4V RETURN
+5.4V
SPARE
SPARE
+20V
20V RETURN
IN +9V REG
9V RETURN SHIELD GRD

FIGURE 24

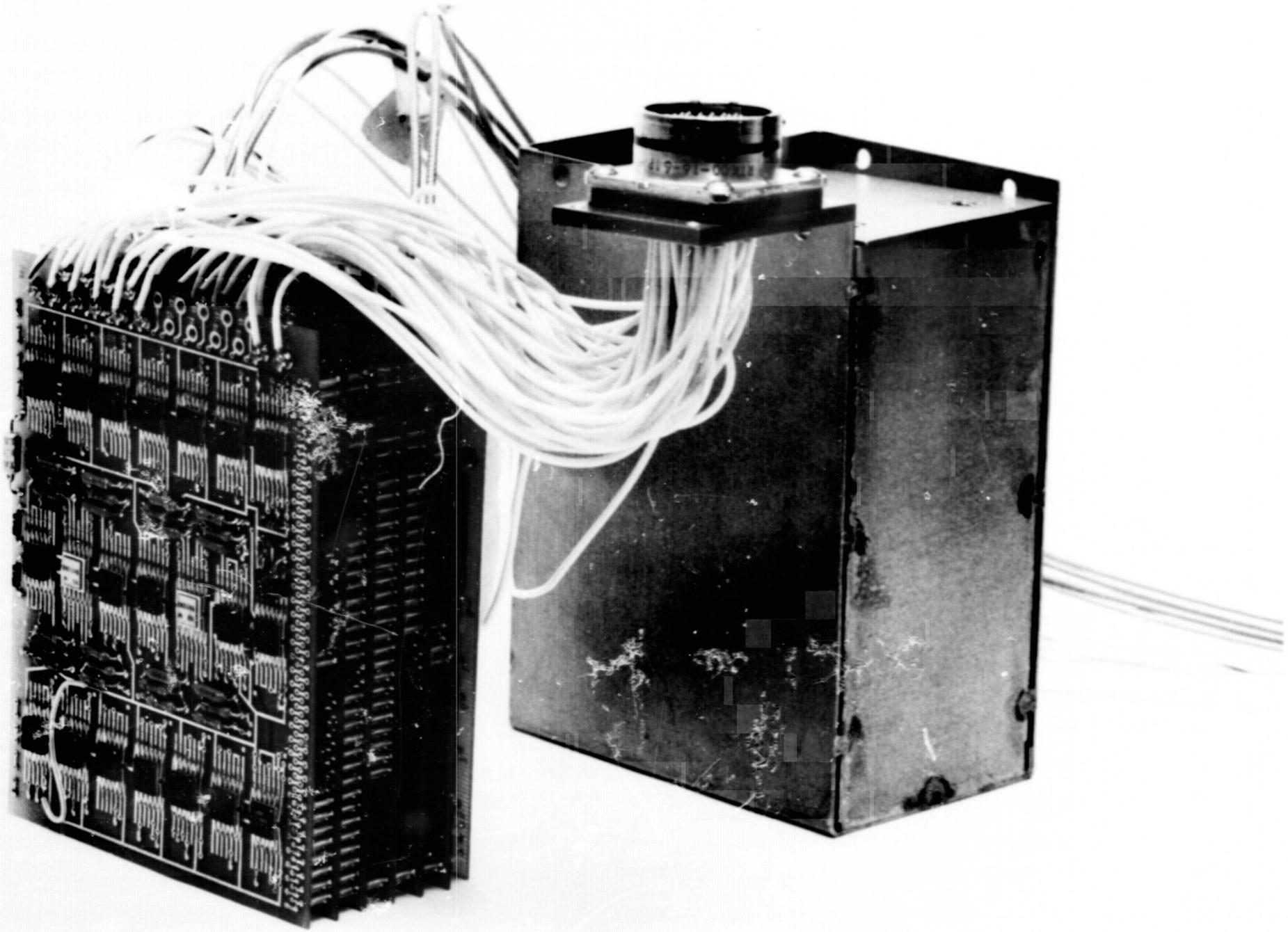


FIGURE 25

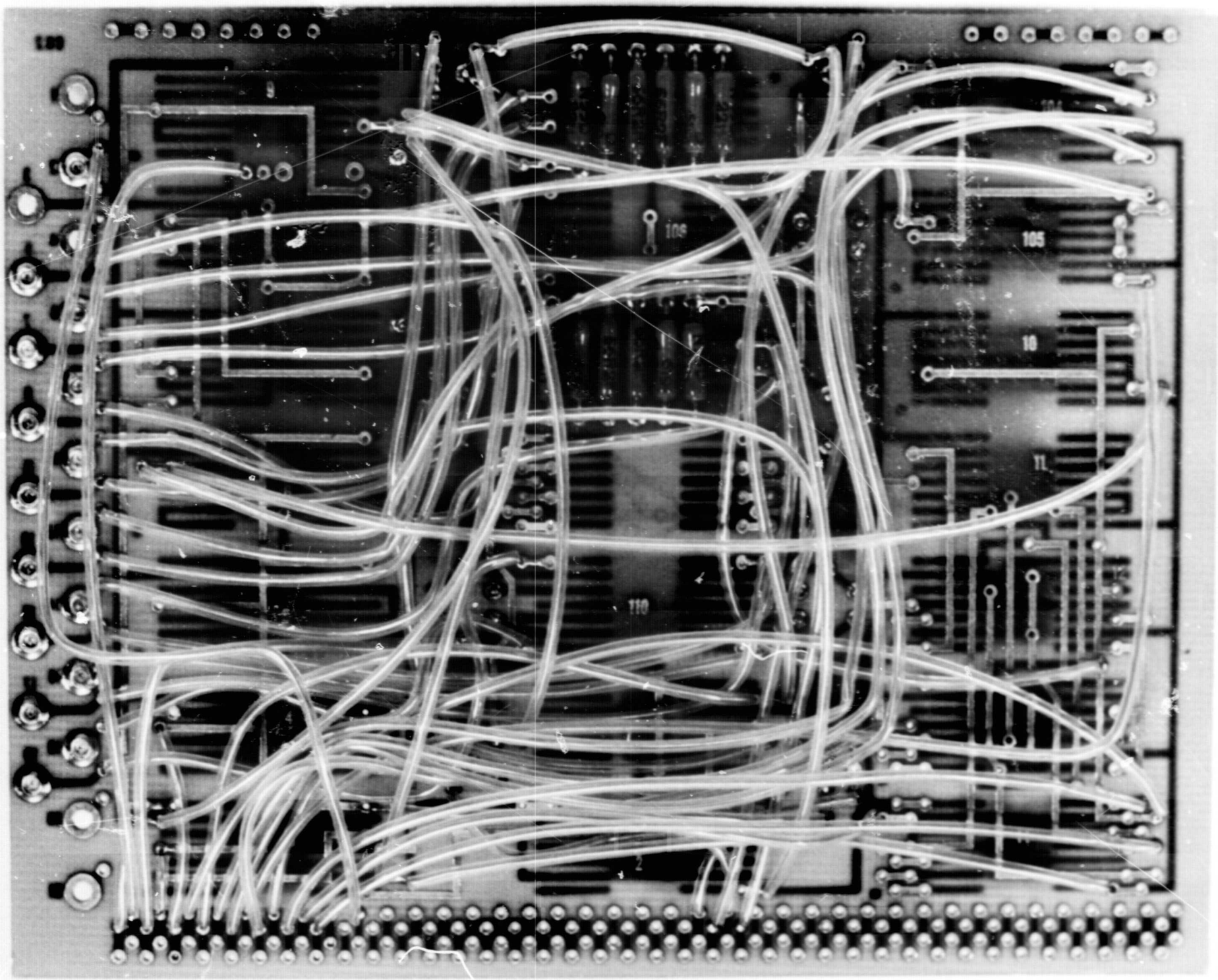


FIGURE 26

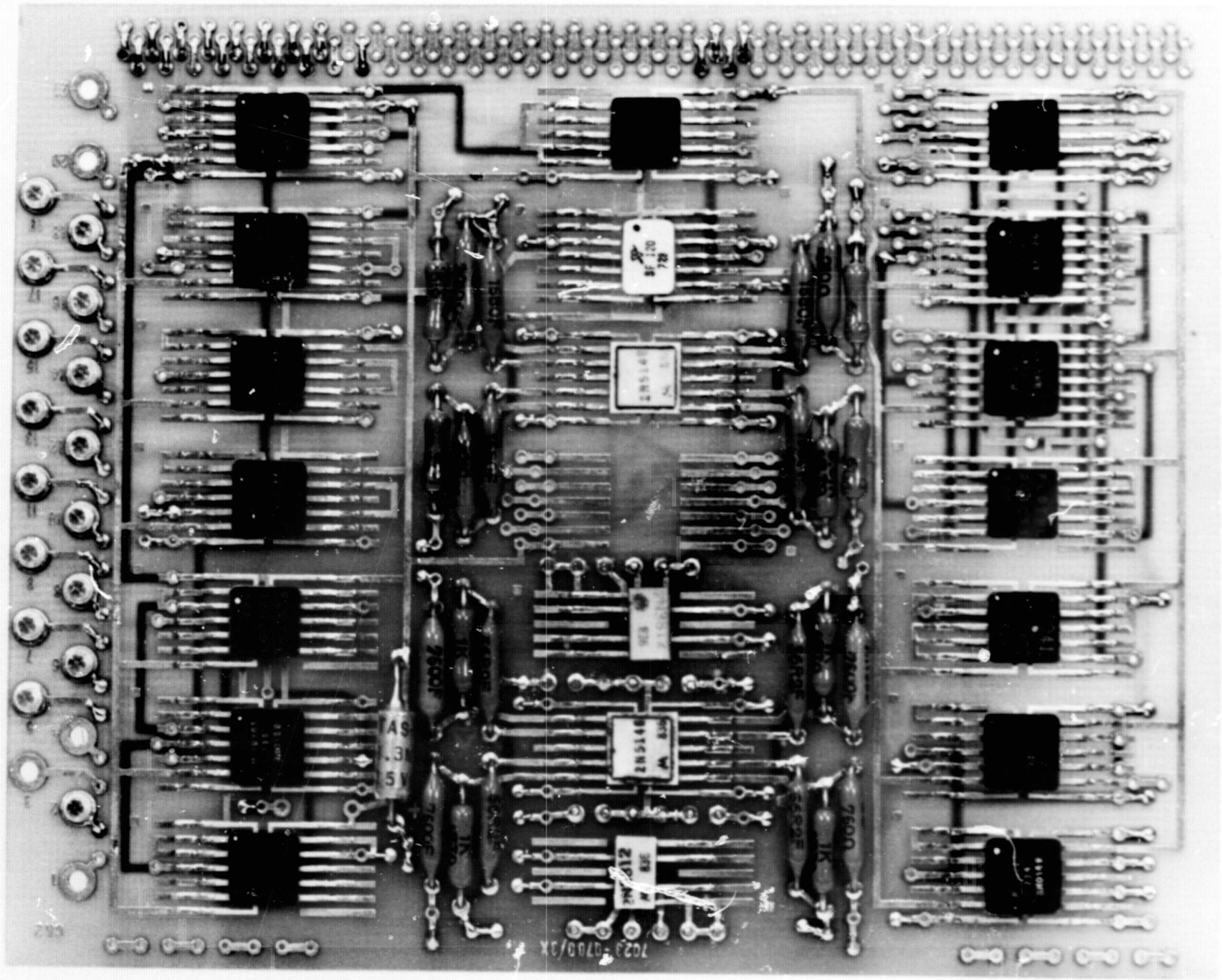


FIGURE 27

2.9.1 INTRODUCTION

General Radio left the logic design of the clock virtually unaltered from the original Varian design. Some consolidation of digital devices to reduce package count was done and a new quad PNP transistor was obtained for the output buffers.

Trouble had consistently been experienced in the clock setting system as it was originally designed for Varian and provided by Varian to Houston. After R. W. Frank's evaluation of June 4, 1968, a new setting logic was developed, designed into the GR clock, and data was transmitted to Houston on December 24, 1968 to permit them to add the setting logic to their test equipment. The balance of this section will describe the functioning of the clock circuits based on the several schematics in sufficient detail to render possible both understanding and maintenance. Figures 25-27 show the final construction techniques used.

2.9.2 GENERAL DESCRIPTION, BASIC BLOCK DIAGRAM

The block diagram 2995-9159-2DC shows the clock in its entirety. The dotted lines segregate this general block diagram as a key to the seven detailed schematic diagrams. The clock is driven (2995-4878-2D) from the RFS crystal oscillator at 8192 kHz. Four binary dividers produce output frequencies at 4096, 2098, 1024, and 512 kHz. The 512-kHz signal is subsequently divided by a factor of 8 to 64 kHz and the 64 kHz is divided by a factor of 10 and buffered to produce the required 6.4 kHz output signal. The 512-kHz signal is also divided by a factor of 2 to produce a separate 256-kHz signal in phase quadrature with the 256-kHz signal driving the scale of 8. The $\overline{64\text{-kHz}}$ signal, in addition to driving the scale-of-10, is first divided by a factor of 2 to produce a 32-kHz signal and

subsequently by another factor of 2 to produce the 16-kHz signal. The 16-kHz signal is divided by 16 to provide the basic $\overline{1\ \text{kHz}}$ which is used to drive the balance of the clock circuits and which is buffered to produce the output 1 kHz.

The 512 kHz, quadrature 256 signal, and 32-kHz signals are combined to form a rate multiplied 800-kHz signal on the clock circuit 1 board (2995-4879-2D). The 800-kHz signal is returned to the clock 2 board for division by 2 to produce 400 kHz. The 400-kHz signal is filtered to remove the combining frequency sidebands on the clock circuit 1 board and this signal is subsequently divided by 4 and buffered to provide the 100-kHz output signal. A scale of 10 shift counter divides the 1-kHz signal to a 100-Hz signal as shown on 2995-4879-2D. Gates associated with this shift counter produce the $\overline{\text{MS2}}$, MS5 and MS8 signals necessary for the IRIG B time code format. The 100-Hz signal, the MS8 signal, and the MS5 signal, are all sent to the clock 3 board (2995-4877-2D) where two additional scales of 10 produce the 1-Hz and $\overline{\text{1-Hz}}$ reference signals. The output of these two decades is further decoded to produce signals required for both IRIG B and IRIG E time code generators.

The 1-Hz signal and those signals necessary for the clock setting system are combined in the setting logic on clock circuit 4 (2995-4876-2D) to drive the decades and scales of 6 providing seconds timing and minutes timing.

Schematic circuit 5 (2995-4873-2D) contains the second block of setting logic and the scale of 24 to produce hours data and the two scales of 10 and the scale of 4 for days information. This circuit system in addition comprises the necessary logic to permit resetting the clock to 0 after either 365 or 366 days to provide for leap year. Again, the output of the scalers is provided in the proper logic sequence to permit connection to the two IRIG time code generators.

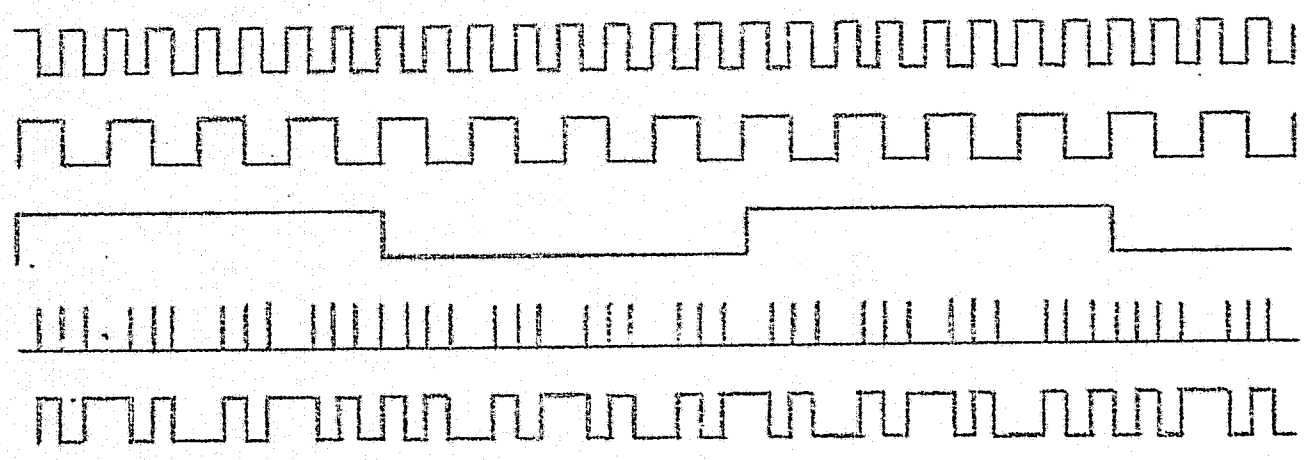
Schematics 6 and 7 (2995-4873-2D and 2995-4875-2D) detail the IRIG B and IRIG E time code generator combining circuits and their buffers.

2.9.3 DETAILED DESCRIPTION, HIGH-FREQUENCY DIVIDERS TO 64 kHz

Clock circuit 2 (2995-4878-2D) shows the 8192-kHz signal reduced to 4096 kHz, 2048 kHz, 1024 kHz, and 512 kHz by IC15A, 15B, IC1A and 1B, respectively. These signals are inverted and buffered by IC106. The Q output of IC1B clocks the 256-kHz quadrature flip-flop (IC104B) and produces the 512-kHz signal for the 800-kHz rate multiplier shown on schematic 1 (2995-4879-2D). The $\overline{Q}$ output of IC1B provides the driving signal for IC2, 3A, and 3B, the 64 kHz divider. The divider clear signal $\overline{\text{CLDIV}}$ resets all flip-flops except the 8192 to 2048 dividers. The 64-kHz signal at the output of IC3B is divided by 10 by the four flip-flops IC7, IC8A, IC8B, and IC9. The $\overline{\text{6.4-kHz}}$ signal is buffered in IC107 to produce the required output signal. IC4A divides the $\overline{\text{64-kHz}}$ signal by 2 producing 32 kHz for the rate multiplier, which signal, in turn, drives IC4B to produce 16 kHz. The 16-kHz signal is divided by 4 in IC5 and by 4 again in IC6 to produce $\overline{\text{1 kHz}}$. This 1-kHz signal is buffered in IC108 to produce the required output signal.

2.9.4 100 kHz SYNTHESIZER

The waveforms of the 512 kHz, 256-kHz quadrature signal and the 32-kHz signal are combined in IC119 and its following adders on drawing 2995-4879-2D to produce a train of positive-going pulses at an average rate of 800 kHz at the output of IC120. For timing, see Figure 28. The resulting 800-kHz signal is returned to the circuit 2 board (2995-4878-2D) for division by 2 to 400 kHz in IC104A and the resulting 400-kHz signal is returned for filtering to the clock circuit 1 board. The filter is comprised of the three field-effect transistors, Q101 through Q103.



WAVEFORMS - 100 KHz SYNTHESIZER
FIG 23

Thirty-two kilohertz sidebands on the 400-kHz signal are reduced to at least 30 dB below the 400-kHz signal by two successive synchronously tuned FET - stages, Q101, Q102. The output 400-kHz signal is buffered by Q103 and returned to the clock circuit 2 board to drive a scale-of-4, IC105. The $\overline{\text{100-kHz}}$ signal from IC105 is buffered for output in IC107.

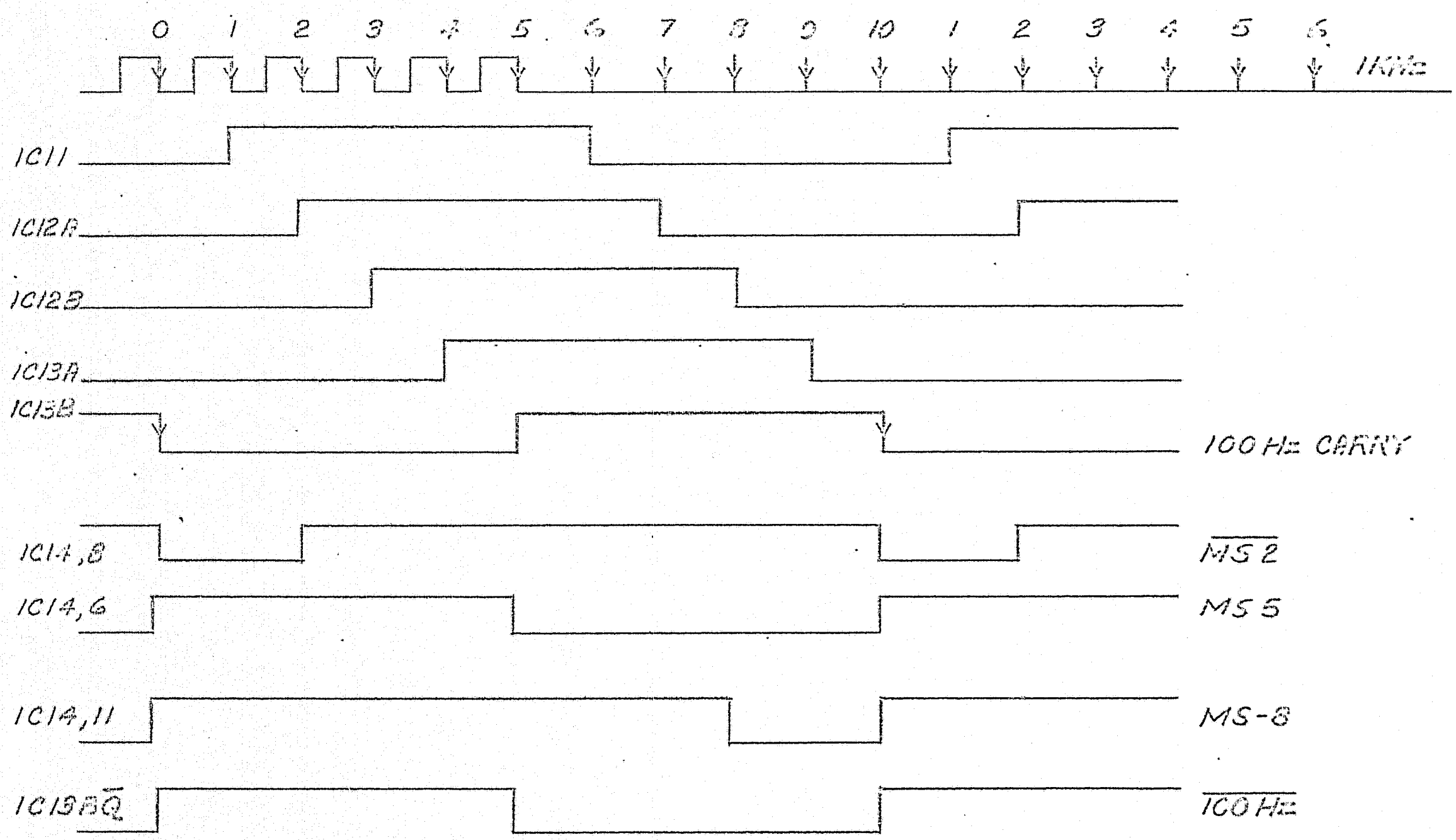
2.9.5 DIVIDERS AND TIME CODE PULSE GENERATORS FROM 1 kHz TO 1 s

The $\overline{\text{1-kHz}}$ signal on clock circuit 2 (2995-4878-2D) is inverted at IC10 and used to drive the first modulo 10 shift counter comprised of IC11, IC12A, IC12B, IC13A, and IC13B. The $\overline{Q}$ output of IC13B directly produces the $\overline{\text{100-Hz}}$ signal fed to the second modulo 10 shift counter on clock circuit 3 (2995-4877-2D). The MS8, MS5 and $\overline{\text{MS2}}$ signals are produced by combining the waveforms of this shift counter. Timing sequences are shown in Figure 29.

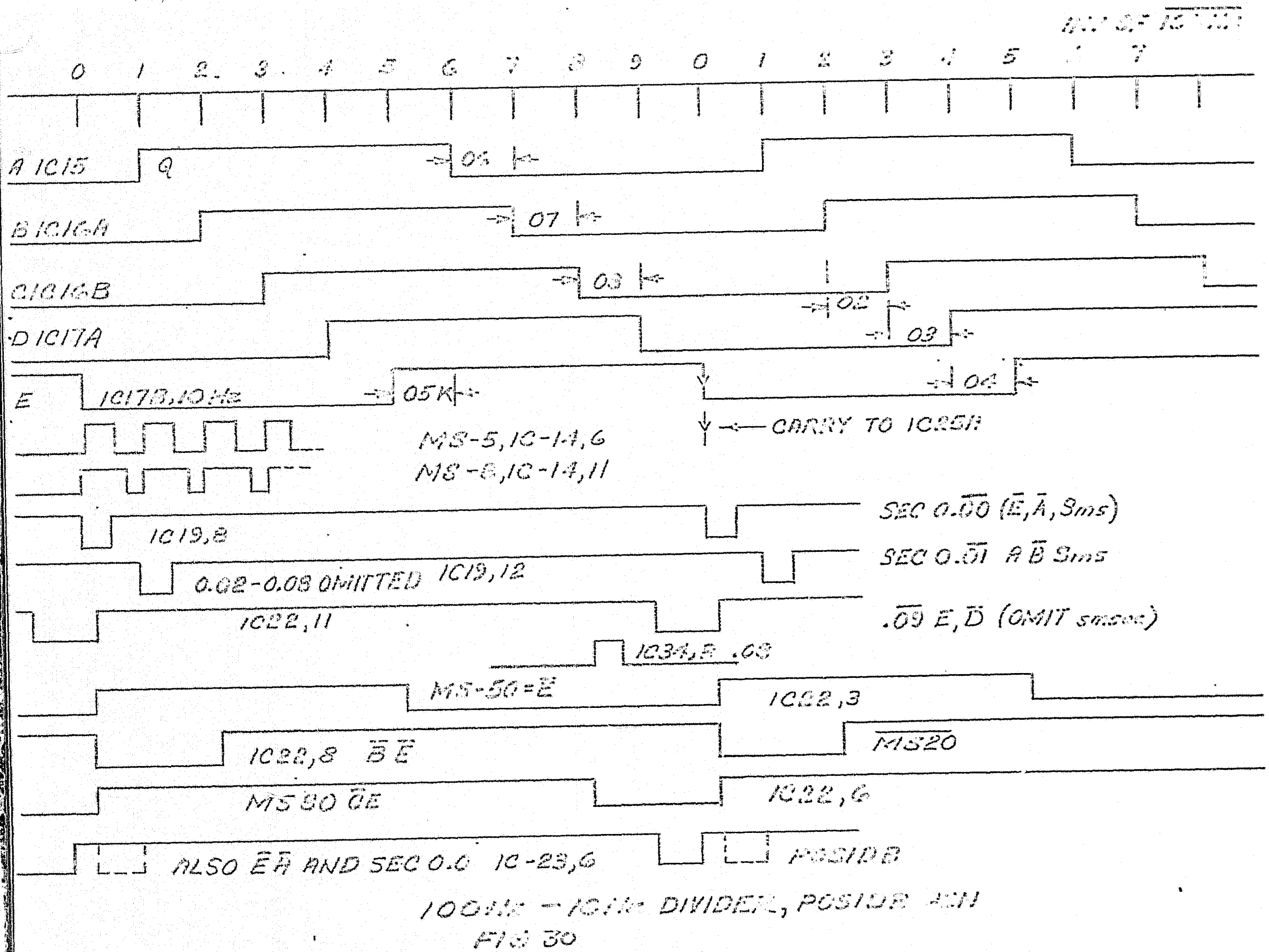
On clock circuit 3 (2995-4877-2D), we begin with the $\overline{\text{100-Hz}}$ signal which is buffered and inverted at IC18 and fed to the second modulo 10 shift counter. This counter produces the 10-Hz output signals. The outputs of this shift counter will combine to produce the 100 pulse per second basic rate for IRIG B, and the 20-, 50- and 80-ms output required for the IRIG E time code.

The $\overline{\text{POSIDB}}$ signal for the IRIG B time code is produced as shown in Figure 30 by combination of the $\overline{A}$, $\overline{E}$, and SEC 0.0 signals in the first "AND" gate of IC28. This signal is combined with $\overline{\text{SEC 0.09}}$ and finally the composite signal is given the proper 8-ms duration by MS8 at pins 4, 5 of IC23.

The "beginning-of-second" pulse SEC 0.0 is high for the first full tenth of a second. $\overline{E}$ and $\overline{A}$ are only high for the first one hundredth second. Thus, pin 8 of IC23 is low for this first hundredth. Pins 2, 13 are normally high. Thus the "first hundredth" will produce an output 1 (positive) signal at



1 KHz - 100 Hz MODULO 10 SHIFT COUNTER
FIG 29



100 Hz — IC-17 DIVIDER, POSIDB HIGH

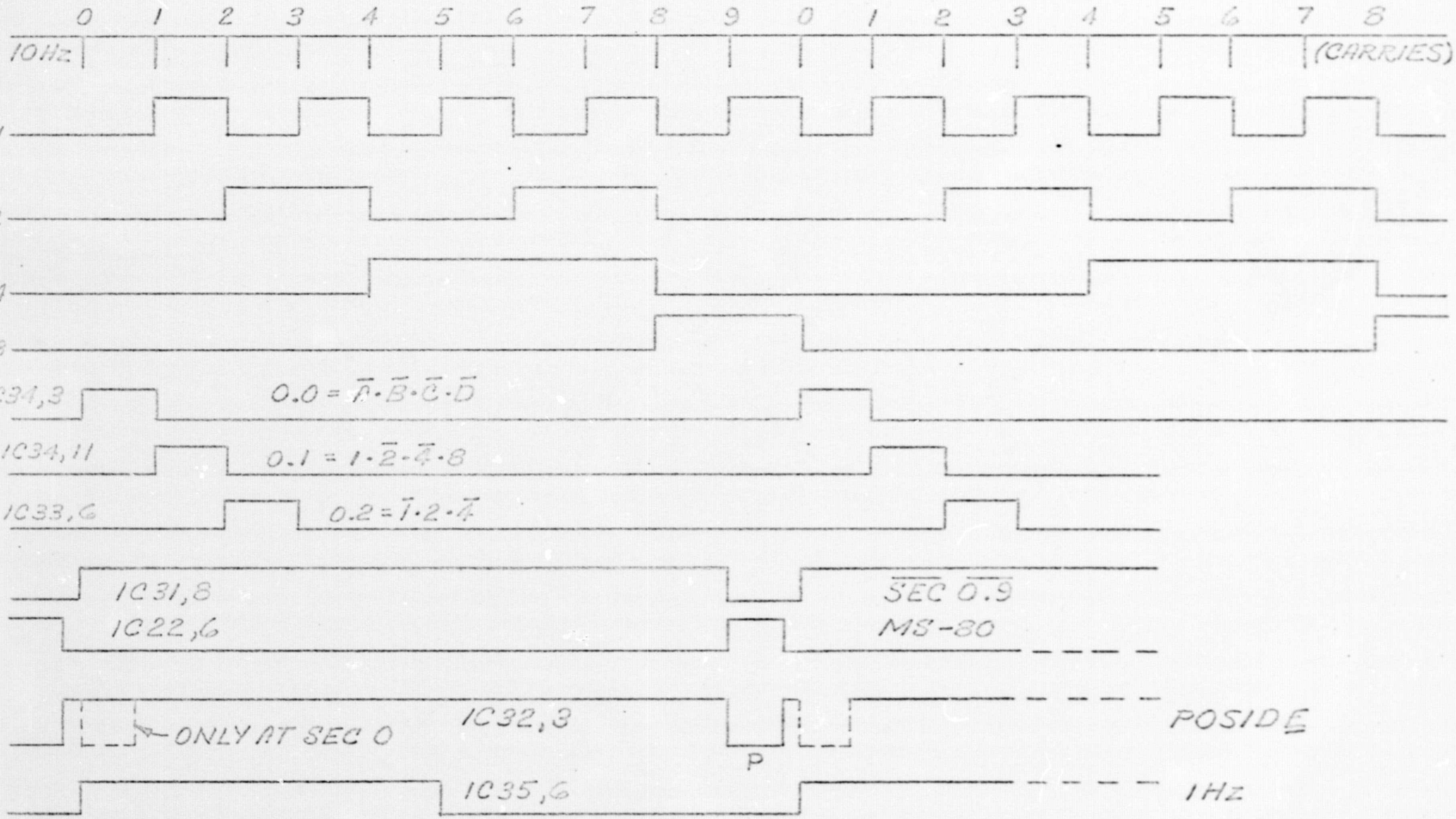
Fig 30

pins 12, 4 of IC23 during the "first hundredth"--and the $\overline{0.09}$ during every interval from 90 to 100 ms. IC23 therefore produces an output signal at pin 6 lasting for 8 ms, both at the beginning of each second, and every tenth-second from 90 to 98 ms--as required for the IRIG B format.

The first 8421 decade reduces the 10-Hz signal to the 1-Hz signal and its complement. Flip-flop IC35 is set to produce the 1-Hz and $\overline{1\text{-Hz}}$ signals from the input 10-Hz clock and the logic states of the decade. The output of the decade is decoded in IC28 through IC34 to produce the seconds 0.0 through 0.8 signals required by the time code generators. The $\overline{\text{SEC 0.9}}$ signal at the output of IC31 and the negative signal produced at either the SEC 0 or SEC 0.0 are combined in IC31 to produce an output signal for IC32 which is subsequently combined in IC32 with MS80 to produce the seconds marker signal, $\overline{\text{POSIDE}}$ for the IRIG E time code generator. These timing sequences and polarities are shown in the timing diagram of Figure 31 and the logic is exactly analogous with that just described above for creating $\overline{\text{POSIDB}}$.

2.9.6 DIVIDERS, 1 s AND 366 DAYS

The seconds and minutes divider chain and their output buffers are shown on the clock circuit 4 schematic (2995-4876-2D). The 8421 decade divides units to tens of seconds. This schematic begins with the first block of clock setting gates (Section 1.9). In the normal operation of the clock, the 1-Hz input signal is inverted by IC39 and passed to the decade. $\overline{\text{INHIB}}$ is normally high. The 16-kHz updating signal is blocked at IC39 because $\overline{\text{FASTC1}}$ is normally high. The seconds and all subsequent scalers are set to 0 by bringing $\overline{\text{CLACC}}$ low.



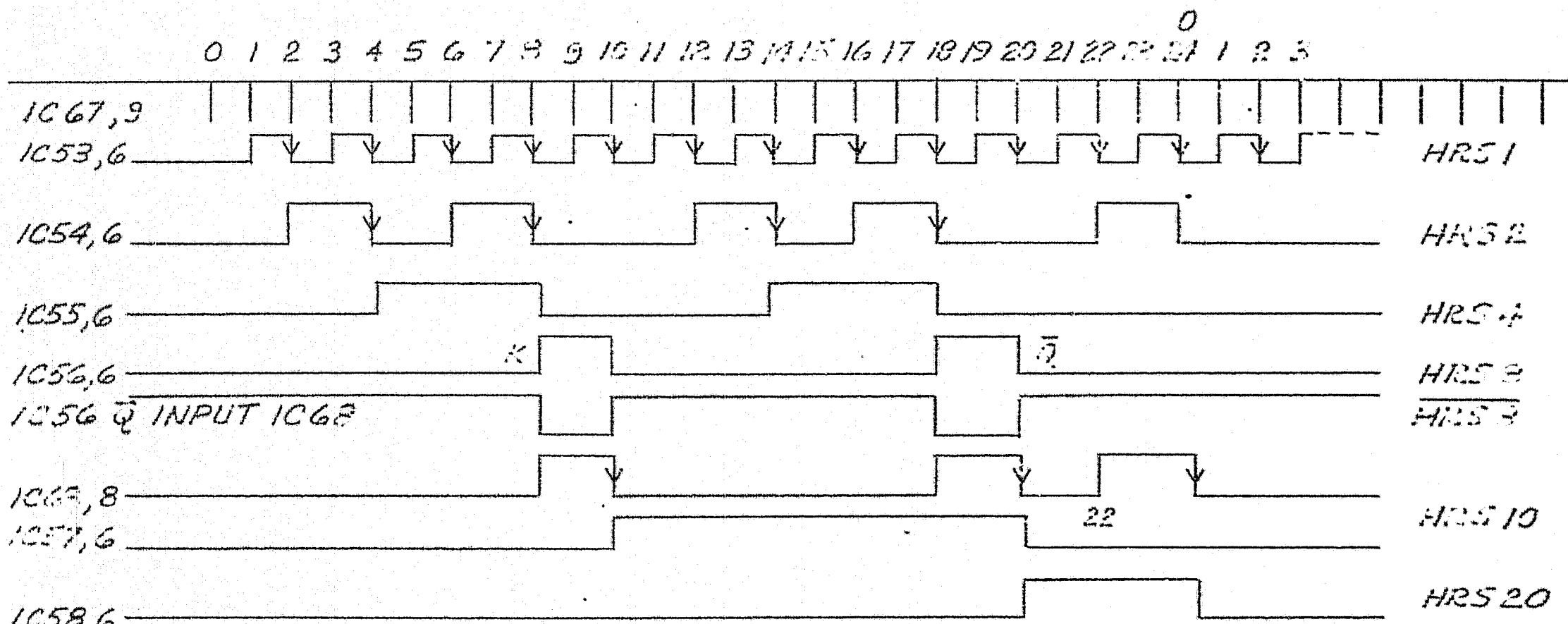
1 SEC DIVIDER, POSIDE GEN
FIG 31

The first decade provides seconds data for the time code generators. The sequential signals, spaced 1 second apart for IRIG E, seconds 0 through seconds 4, are provided by combining the decade output states in IC's 40 through 42. Straight binary data SEC B1 through B8 and $\overline{\text{SEC B1 through B8}}$ are provided directly from the IC's of the decade.

The divide by 6, producing tens of seconds, is comprised of IC's 44 through 46. This scaler produces the signals SEC 10, 20, 40 and $\overline{\text{SEC 10, 20, 40}}$. The complement outputs are buffered for direct output and the direct signals are sent to the time code generators on circuits 6 and 7. In an exactly analogous system, the signal once per minute at the output of IC46 is divided in a decade and a scale of 6 to a signal at once per hour. The units of minutes and tens of minutes and their output complements are produced in IC47A through IC52, buffered for output and passed to the time code generator in a fashion exactly analogous to the seconds data above.

The hours and days scalers and their buffers are shown on clock circuit schematic 5 (2995-4873-2D). The hours scalers are shown preceded by the second block of fast update logic comprised of IC's 67 and 68. Normally, the $\overline{\text{MIN40}}$ signal is passed by IC67. The balance of the update logic will be described in Section 2.9.9.

The timing sequence for the 24-hour scaler is shown in Figure 32. This scaler is comprised of IC's 53 through 58 and the associated gates of IC68. The timing and gating sequence is complex and will consequently be described in detail following the timing diagram. Initially, all of the flip-flops are in the $\overline{Q}$ state (terminal 9 high). The flip-flops clock on negative input transitions. IC53, the "hours" flip-flop, complements normally and continuously. IC54 is permitted to complement normally only so long as IC56 has terminal 9 high. It



24 HOUR SCALER TIMING
FIG 32

will, therefore, be inhibited when the HRS8 is high. IC55 is permitted to complement except when HRS20 is high (IC58 in the Q state). Under these circumstances, IC's 53 through 56 operate as a normal scaler for HRS1 through HRS8. IC56 is in the Q state and IC54 is therefore inhibited at 10 hours. At the tenth hour, the Q to $\overline{Q}$ transition of IC53 will clock IC56 from Q to $\overline{Q}$ and the positive transition at pin 9 of IC56 will pass IC68, be inverted to a negative transition, and move IC57 to its Q state. Since IC56 is now in $\overline{Q}$, the inhibit is removed at pin 13 of IC54 and IC54 is again free to complement. IC54 complements at hours 12 and 14 and the transition from Q to $\overline{Q}$ at hour 14 again carries to IC55. At hour 18, the Q to $\overline{Q}$ transition of IC54 carries IC55 Q to $\overline{Q}$ and again sets IC56, which, in turn, reapplies the inhibit to IC54 and at the same time produces a carry through IC68 to IC57 moving it from its Q to its $\overline{Q}$ state and carries to the HRS20 flip-flop. The HRS20 flip-flop now applies its inhibit to IC57, which will hold it at its original $\overline{Q}$ state and to IC55 which will hold it at its $\overline{Q}$ state. At the same time, the HRS20 signal at pin 6 of IC58 enables pin 4 of IC68. Now, finally, at the 24th hour IC54 in making its transition from Q to $\overline{Q}$ will bring pin 5 of IC65 low, pin 6 of IC68 will go high, pin 8 low, and IC58 will be returned to the $\overline{Q}$ state. All IC's have now returned to the $\overline{Q}$ state and the process is ready to repeat.

The negative transition of the HRS20 line occurring at the 24th hour is applied to the days scaler. Days and tens of days are accumulated in two 8421 decades comprised of IC's 59 through 64. The output of the tens of days scaler is accumulated in a scale of 4 comprised of IC65. The days clock is reset to 0 at the end of day 364 or at the end of day 365, to allow for leap year. Let us assume that the clock is to accumulate for a normal year. IC66 will be set by the $\overline{FS365}$ signal to the Q state. Pin 1 of IC69 will be high. The $\overline{Q}$ signal from

IC66 at pin 13 of IC69 holds pin 11 high. Therefore, IC69 pin 8 will be high or low depending upon the state of the DAYS1 signal, going high at day 1, 11, etc. The output of IC69 at pin 8 is applied at IC70 which has its "extender" terminals at pins 3 through 11 connected so that it makes a 6 high "AND" gate combining DAYS1 with DAYS4, 20, 40, 100, and 200. Therefore, at day 365, all inputs go high and the days full scale reset line goes low. This signal applies a set at pin 11 of IC121. IC121's $\overline{Q}$ signal now goes low and the output of IC68 at pin 3 becomes high, is inverted to IC69, to produce a clear signal resetting all of the days scalers. Note that pin 2 of IC68 is normally high. Therefore, $\overline{\text{CLACC}}$ will normally pass IC68 and be inverted by IC69 to produce the standard clear signal. The end-of-year clear signal produced by IC121 is terminated by the next negative transition of 16 kHz. The sequence at leap year is identical in principle to that just described. Flip-flop IC66 is set to the $\overline{Q}$ state rather than the Q state by $\overline{\text{FS366}}$ and the DAYS2 signal in going high at pin 12 of IC69 initiates the clear sequence.

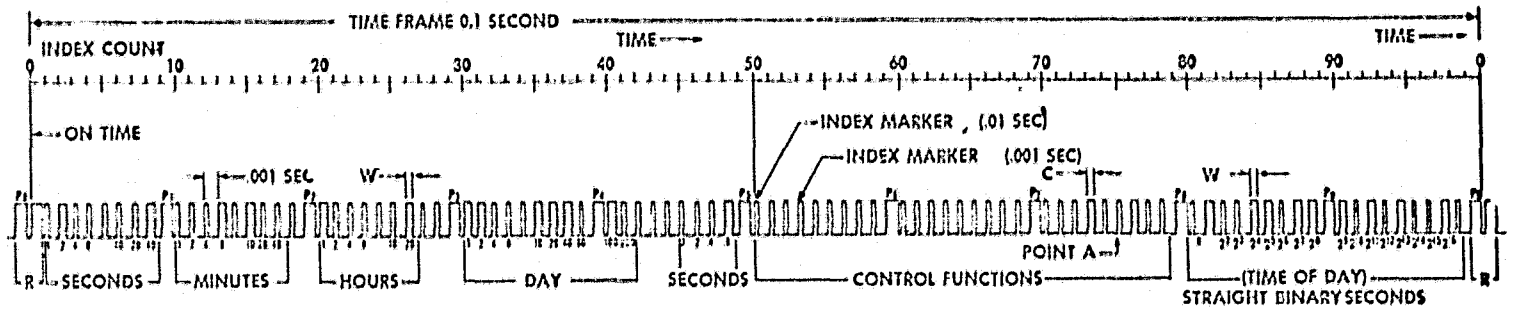
2.9.7 IRIG B TIME CODE GENERATOR

The combining gates and buffers of the IRIG B time code generator are shown on clock circuit 6 (2995-4875-2D). The logic may be best understood by beginning at the output. It is suggested that the reader refer frequently to the standard IRIG B time code format (Figure 33.) and to Figure 30. The IRIG B signal at IC116 pin 7 is a positive-going waveform. The output at pin 2 of IC86 must therefore also be positive going. The input at pins 4, 5, and 6 of IC58 will normally be high. Its output at pin 2 will therefore go high when any one of the input pins are low. A 2-ms output pulse train at the 100-pps basic rate is therefore produced by $\overline{\text{MS2}}$. These 2-ms duration pulses serve as sync and the basic binary 0 information for the code. Refer now to Figure 30. The normal

IRIG TIME CODE FORMATS

FORMAT A

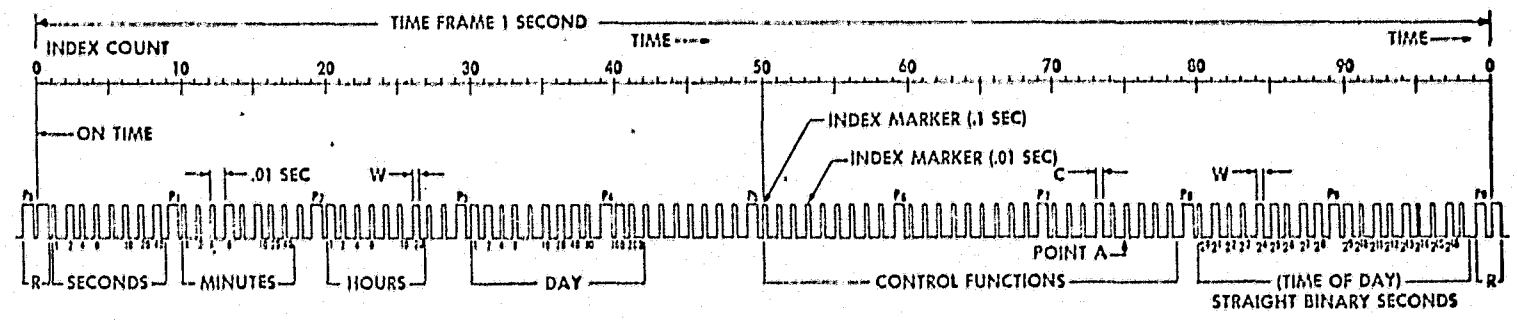
1000-PPS, 34-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A 21:18:42 + .8 + .07 + .005 21 HR, 18 MIN, 42.875 SEC. ON DAY 173

FORMAT B

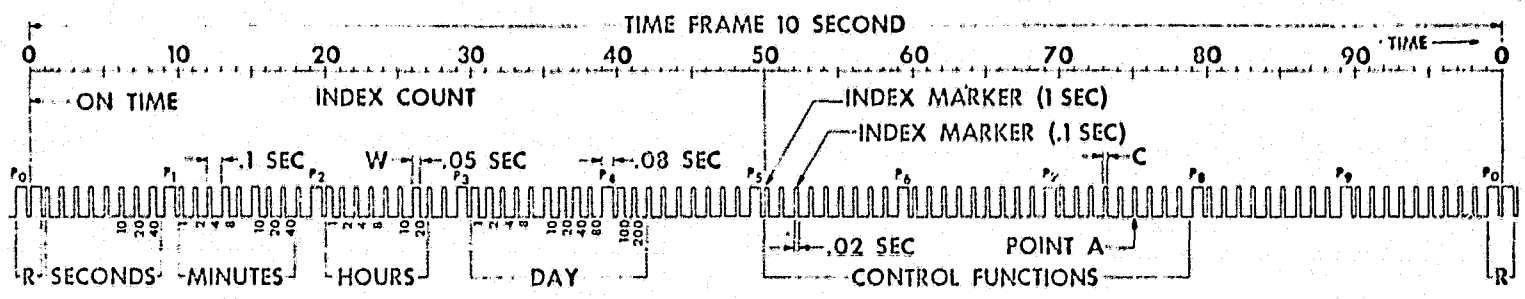
100-PPS, 30-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A = 21:18:42 + .7 + .05 = 21 HRS. 18 MIN. 42.75 SEC. ON DAY 173

FORMAT E

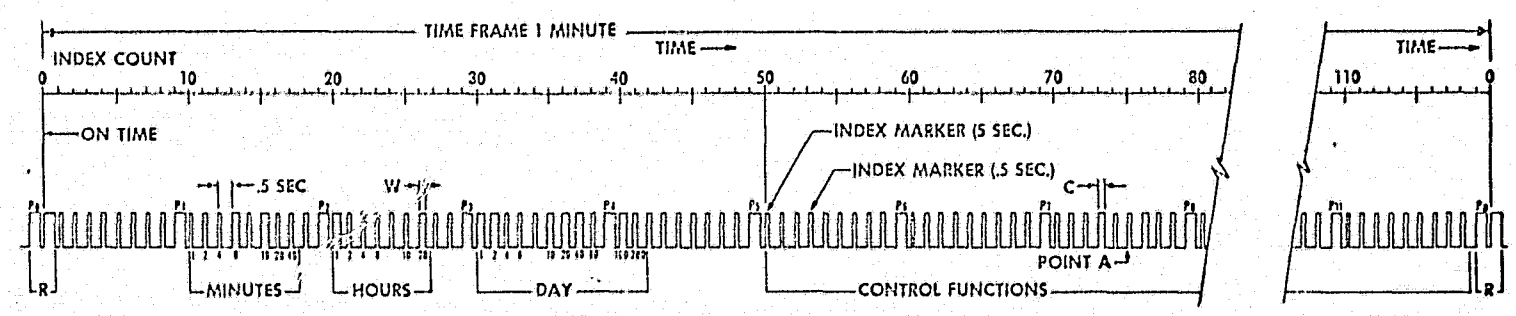
10-PPS, 26-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A = 21:18:40 + .7 + .5 = 21 HR.18 MIN. 47.5 SEC. ON DAY 173

FORMAT C

2-PPS, 23-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A = 21:18 + 37.5 SEC. = 21 HRS. 18 MIN. 37.5 SEC. ON DAY 173

Code Format	Ref. Mark "P"	Binary "1" and W and C	Binary "0" and Index Marker
IRIG A	0.8 ms	0.5 ms	0.2 ms
IRIG B	8 ms	5 ms	2 ms
IRIG C	0.4 sec	0.25 sec	0.1 sec
IRIG D	48 sec	30 sec	12 sec
IRIG E	80 ms	50 ms	20 ms

FIG 33

"P" marker pulse is produced by $\overline{\text{POSIDB}}$ between .09 and .098 s, the second 0 marker is added to this signal by combining the SEC 0.0 at pin 10 of IC23 on clock circuit 3 schematic (2995-4877-2D).

The time code binary 1 data in the IRIG B format has a duration of 5 ms. Note on Figure 30 that the $\overline{\text{SEC 0.00}}$, $\overline{\text{SEC 0.01}}$, etc., signals are produced with 5-ms duration. These signals are inverted by IC102 and IC103 and are positive going.

Now that the basic sync format has been developed, let us study the logic of adding data to the signal. A data "ONE" is represented by broadening a basic 2-ms sync pulse to 5 ms. The pulses at the massive "OR" are low for this duration. In IRIG B format the data is carried by pulses 0.00 through 0.08 (inputs to inverters IC102 and IC103). These signals have 5-ms duration. Now in the first tenth second (SEC 0.0), the seconds data are transmitted. IC71, 72, 73 and 74 are enabled by SEC 0.0 for this data block. Note that in this first block, the 5-ms pulse SEC 0.00 is not used due to the presence of the "on time" frame-sync pulse. Let us suppose that the time at the beginning of the example is 37 seconds. The data will be SEC B1, SEC B2 high, SEC B4 high (7 seconds) and SEC 10, SEC 20 high (30 seconds). After the fram marker, 5-ms duration pulses will appear, sequentially, as a low voltage at the output "OR" on the first, second, and third pulses representing units. Note that the fifth pulse (SEC 0.05) is never used in this block. Now the tens of seconds are next encoded as 5-ms duration pulses at positions 6 and 7 representing 30. The second tenth-second time block from 0.2 to 0.3 second carries information about minutes. Here, the fifth pulse (SEC 0.05) is used to carry tens of minutes. The time from 0.00 to 0.01 carries units of minutes. (IC74 pins 11, 12, 13. From 0.01 to 0.02 two's minutes, etc.) In this time block, units and minutes data is separated from 10's minutes by the sync pulse at 0.04 second which is never used.

2.9.8 IRIG E TIME CODE GENERATOR

The IRIG E time code generator is similar to that for the IRIG B format just described except that in this format the bit rate is 10 pulses per second, the "binary 0" is 20 ms in duration and a "1" bit has a duration of 50 ms. The SECS 0.0 through 0.8 signals are not formed to a 50-ms duration in a fashion parallel to that of the IRIG B generator. The bit duration of 50 ms is supplied to the input of IC100 at pin 11 by MS50. Time of day data information at the massive "OR" input of IC100 will be represented as a negative signal. Positive output of IC100 will combine with MS50 to produce a 50-ms negative output at pin 9 of IC100. Any negative input at 4, 5, or 6 of IC101 will produce a positive output at pin 2 and will be inverted to produce $\overline{\text{IRIG E}}$ at pin 9. The normal 10 pulse per second 20 ms duration, sync signal is produced at pin 5 of IC101 by $\overline{\text{MS20}}$ and the 1-second frame sync signal $\overline{\text{POSIDE}}$ at pin 6 is produced in a method analogous to that of POSIDB as shown in Figure 31.

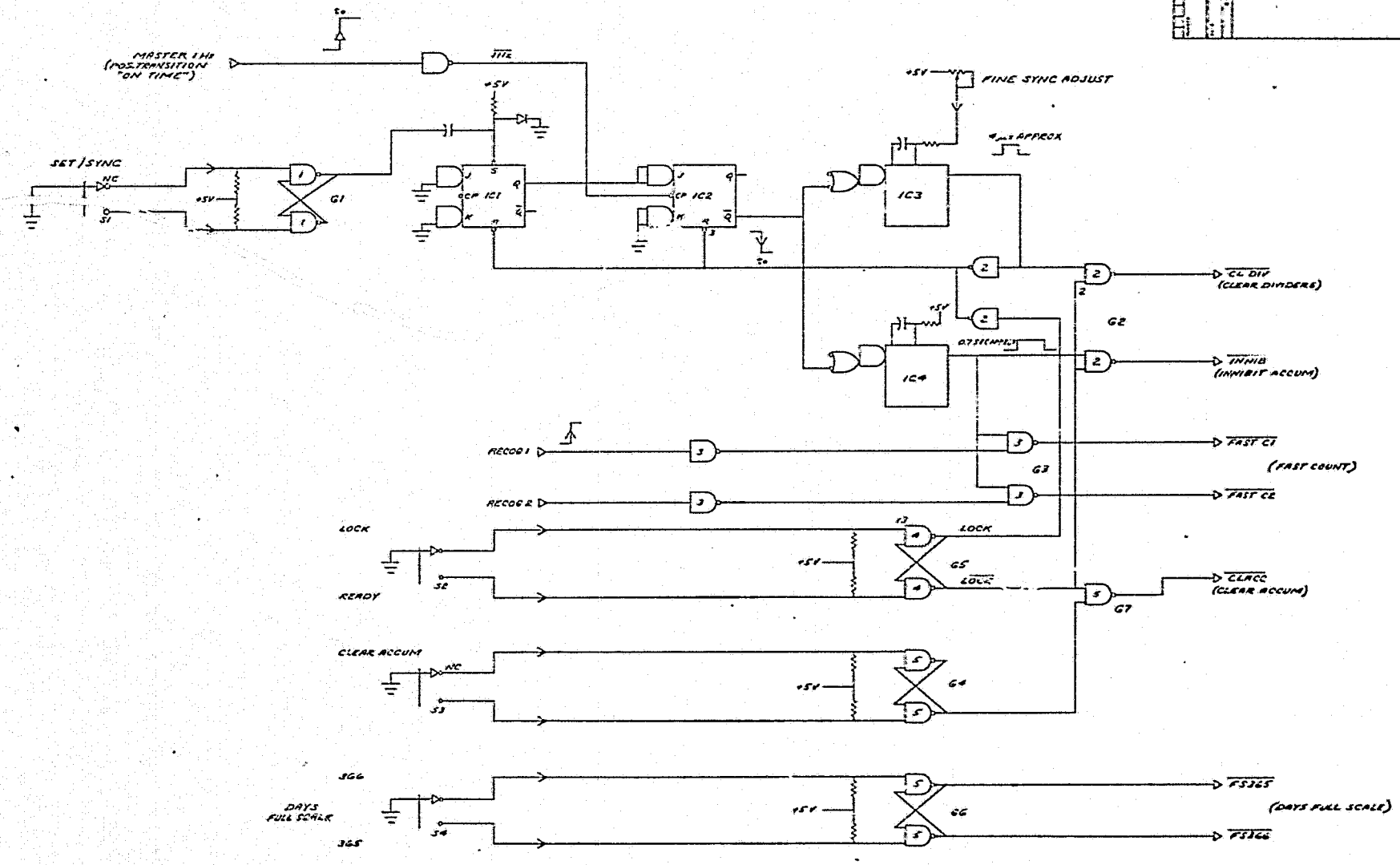
Referring now to the format E time code diagram of Figure 33, let us study the application of data to the basic sync format just developed. Remember the basic sync frame lasts ten seconds. Units of seconds is therefore carried by sync. Let us assume, as with the past example that it is 30 seconds past something. Tens of seconds and twenties of seconds are again high. The first data block (SEC 0.1 SEC 1) contains only 10, 20, 40 SEC at SEC 0.6, 0.7, 0.8, respectively. Thus, in this block the massive "OR" goes negative at the sixth and seventh pulse. The second block, SEC 1-2, carries minutes data, SEC 0.0, MIN 1, SEC 0.1 carries MIN 2, etc. Note that the fourth pulse is never modulated but is used as a separator. SEC 0.5 in this frame carries tens of minutes information, SEC 0.6, 20's, etc. The reader may now carry on the example as desired.

2.9.9 FAST UPDATE CLOCK SETTING SYSTEM

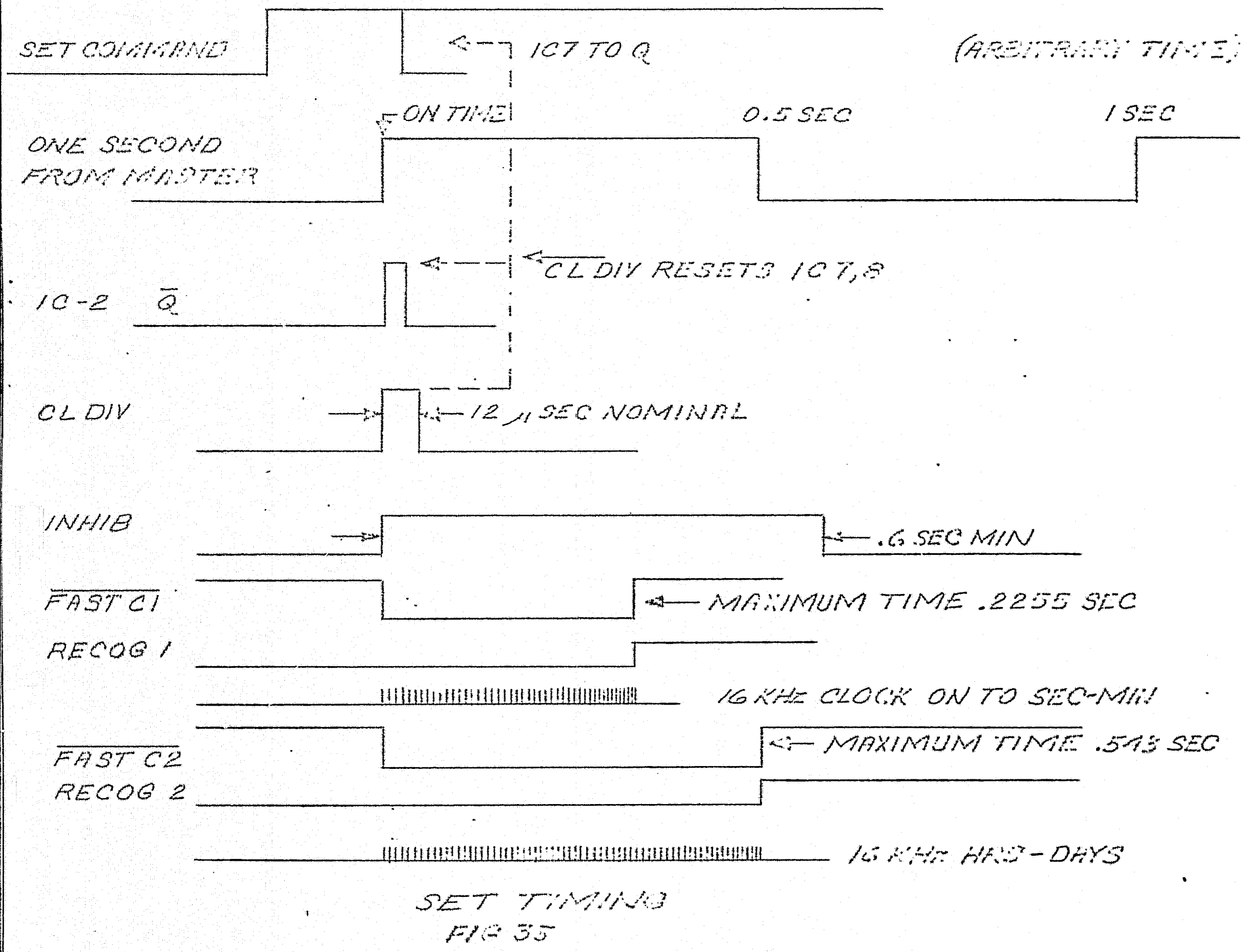
As we have previously mentioned in the Introduction, principles in the original Varian prototype led, in late 1968, to a redesign of the clock setting logic. In the original design, the entire time of day clock from units of seconds onward was updated by slewing at the 100-kHz rate requiring a time as long as 6 minutes to fully set the clock. The new clock setting logic permits a fast update in less than 1 second by separating the clock into two counting blocks. The first from seconds to hours and the second from hours into the days to 365.

A block diagram of the clock setting logic external to SATS is shown in Figure 34. Timing is shown in Figure 35. The sequence is initiated by a SET/SYNC command (the accumulator clear $\overline{\text{CLACC}}$ is optional). Such a command can only be given by moving the LOCK/READY switch to "READY" to bring pin 13 of gate 5 high. The LOCK/READY switch must be placed in the "READY" position to begin the update sequence with the SET/SYNC switch. $\overline{\text{LOCK}}$ will then go high to permit $\overline{\text{CLDIV}}$ and $\overline{\text{INHIB}}$ to go low at the appropriate times.

Let us now suppose that the LOCK/READY switch has been moved to "READY" and the SET/SYNC switch is set to SYNC. At this time IC1 will set to Q, enabling the "J" input of flip-flop IC2, which will go to Q on the next positive transition of the master clock's 1-Hz signal. The negative transition at pin 9 of IC2 will trigger monostable multivibrators IC3 and IC4. Since pin 2 of gate 2 is already high due to the READY signal, $\overline{\text{CLDIV}}$ will go low setting all dividers up to 1 second to proper states for clock synchronization. This signal also resets IC1 and IC2 to their $\overline{Q}$ states. IC4 generates a time interval of approximately 0.7 seconds (it must be over 0.6 second in duration) which, inverted at pin 6 of gate 2, produces the negative inhibit signal stopping the normal 1-second and 1-hour carries to the accumulators.



SATS TIME SET PROGRAM
FIG. 34

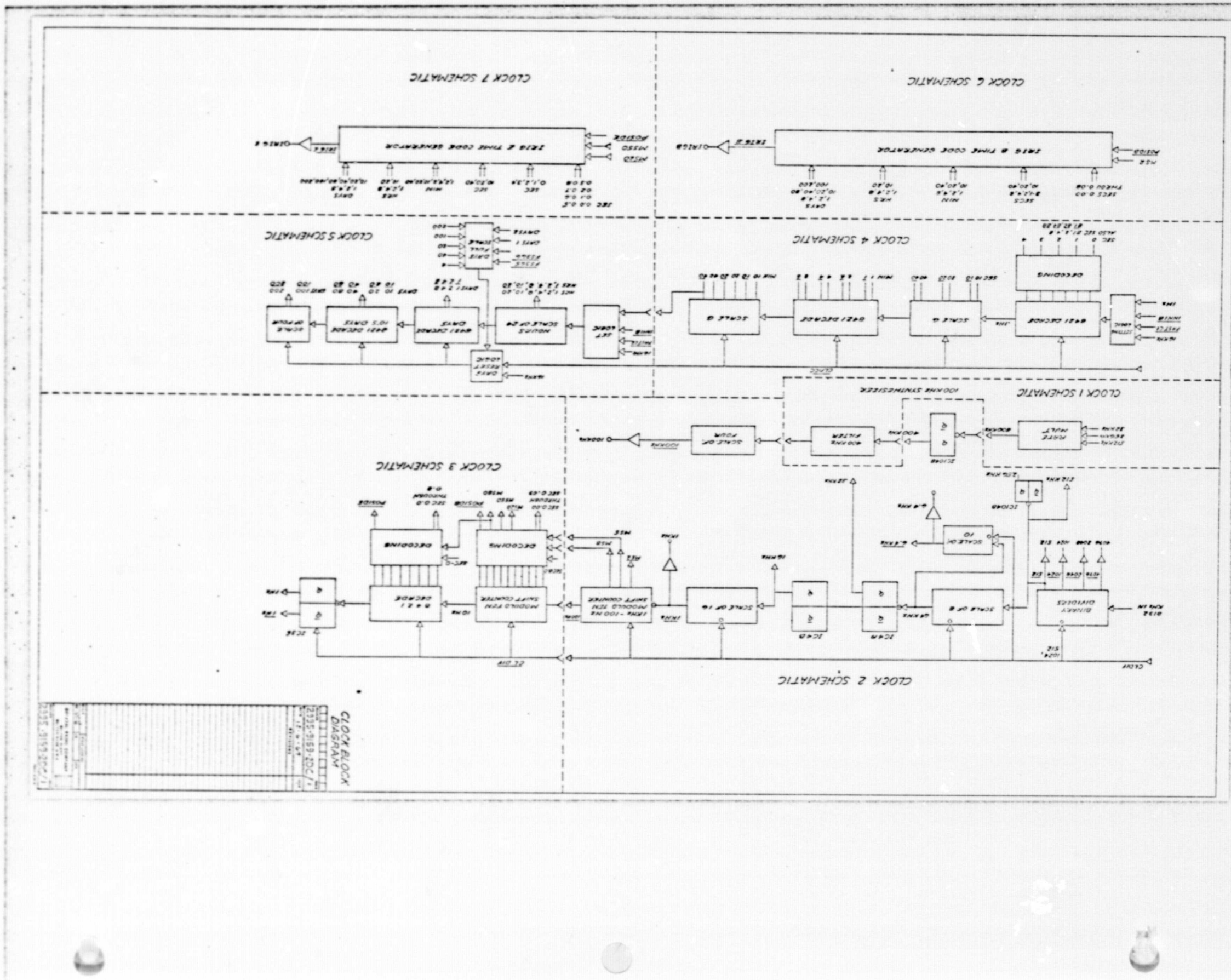


SET TIMING
FIG 35

As stated in the last paragraph, monostable multivibrator IC3 producing the nominal "4-μs" $\overline{\text{CLDIV}}$ signal holds all dividers in their "cleared" states. This cleared state is not all zeroes. Note that, on clock schematic 2 (2995-4878-2D) IC1A, IC1B and IC2 are held in their Q states by the $\overline{\text{CLDIV}}$ signal. Note also that the carries from IC3A and IC3B come from their $\overline{Q}$ sides rather than the usual Q side. With this arrangement, the first input pulse of 2048 kHz from IC15B will immediately change the states of IC3A through IC3B and issue a carry pulse to IC14A. If these flip-flops had been wired for normal dividers, then very nearly 15 μs would have elapsed before a carry was produced for IC4A.

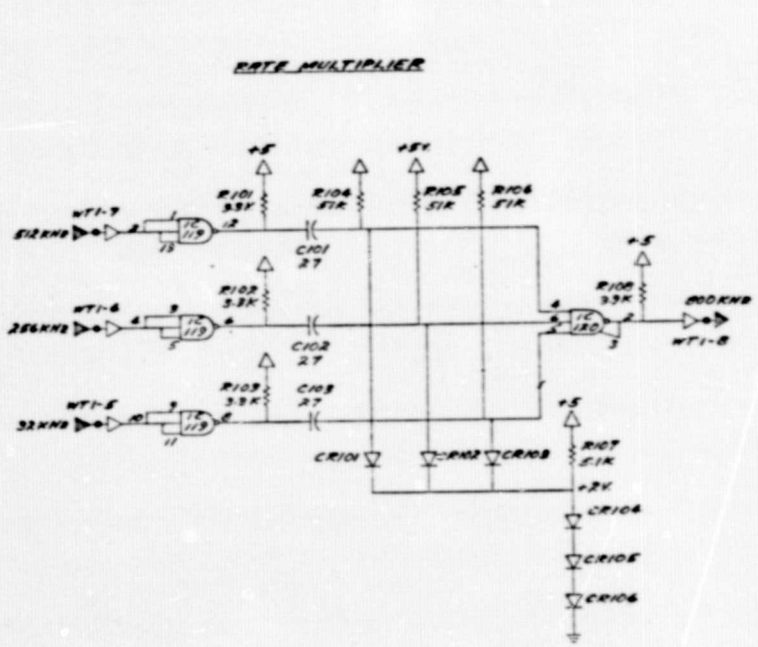
The SATS clock, in the absence of flip-flop time delays, would be fast by 11 μs if the $\overline{\text{CLDIV}}$ has a duration of 4 ms. Allowing a propagation delay of 0.1 μs per flip-flop from IC4A on to the 1-Hz output pulse, an additional delay of 2 μs may be expected. Theoretically, therefore, if the $\overline{\text{CLDIV}}$ pulse is 4 μs then the SATS should, as now instrumented, be set about 9 μs fast. $\overline{\text{CLDIV}}$ should be increased in duration to permit proper, exact setting.

When the inhibit output at pin 8 of IC4 is high and RECOG lines are low, $\overline{\text{FASTC1}}$ and $\overline{\text{FASTC2}}$ go low. These signals are applied to the two update logic systems in the SATS. Let us go to the 1-Hz input system on clock circuit 4 (2995-4876-2D). $\overline{\text{FASTC1}}$ going low at 12 of IC43 enables IC39 and the 16-kHz signal is passed. The seconds, minutes, decades now rapidly slew until a time is reached which is the same as that of the master clock. When recognition is received, RECOG goes high and $\overline{\text{FASTC1}}$ returns positive. The hours, days block operates independently in exactly the same fashion.

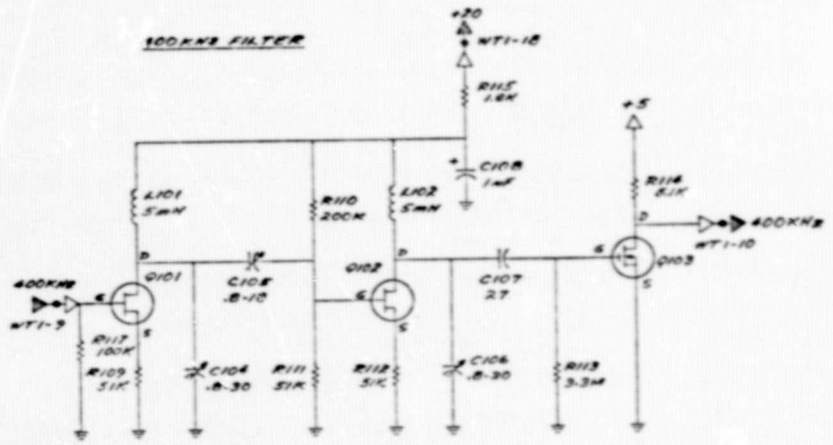

CLOCK 6 SCHEMATIC
CLOCK 7 SCHEMATIC
CLOCK 4 SCHEMATIC
CLOCK 5 SCHEMATIC
CLOCK 1 SCHEMATIC
CLOCK 3 SCHEMATIC
CLOCK 2 SCHEMATIC
CLOCK BLOCK DIAGRAM

CLOCK CIRCUIT #1

RATE MULTIPLIER



100 KHZ FILTER



NOTE:
IC 119, 120 +5 CONNECTED TO PIN 14
GND CONNECTED TO PIN 7

CLOCK CIRCUIT-2

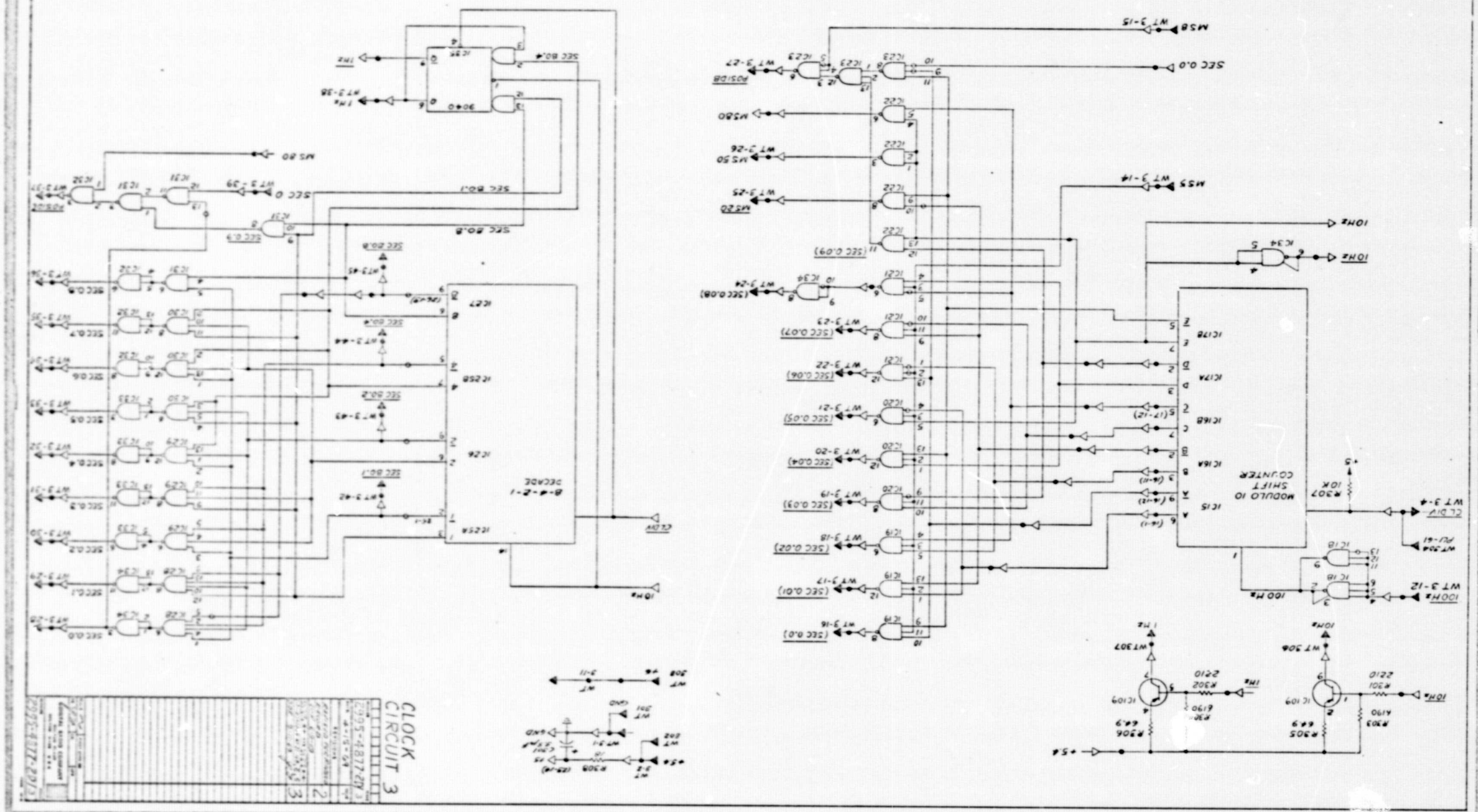
SYNTHESIZER DIVIDERS

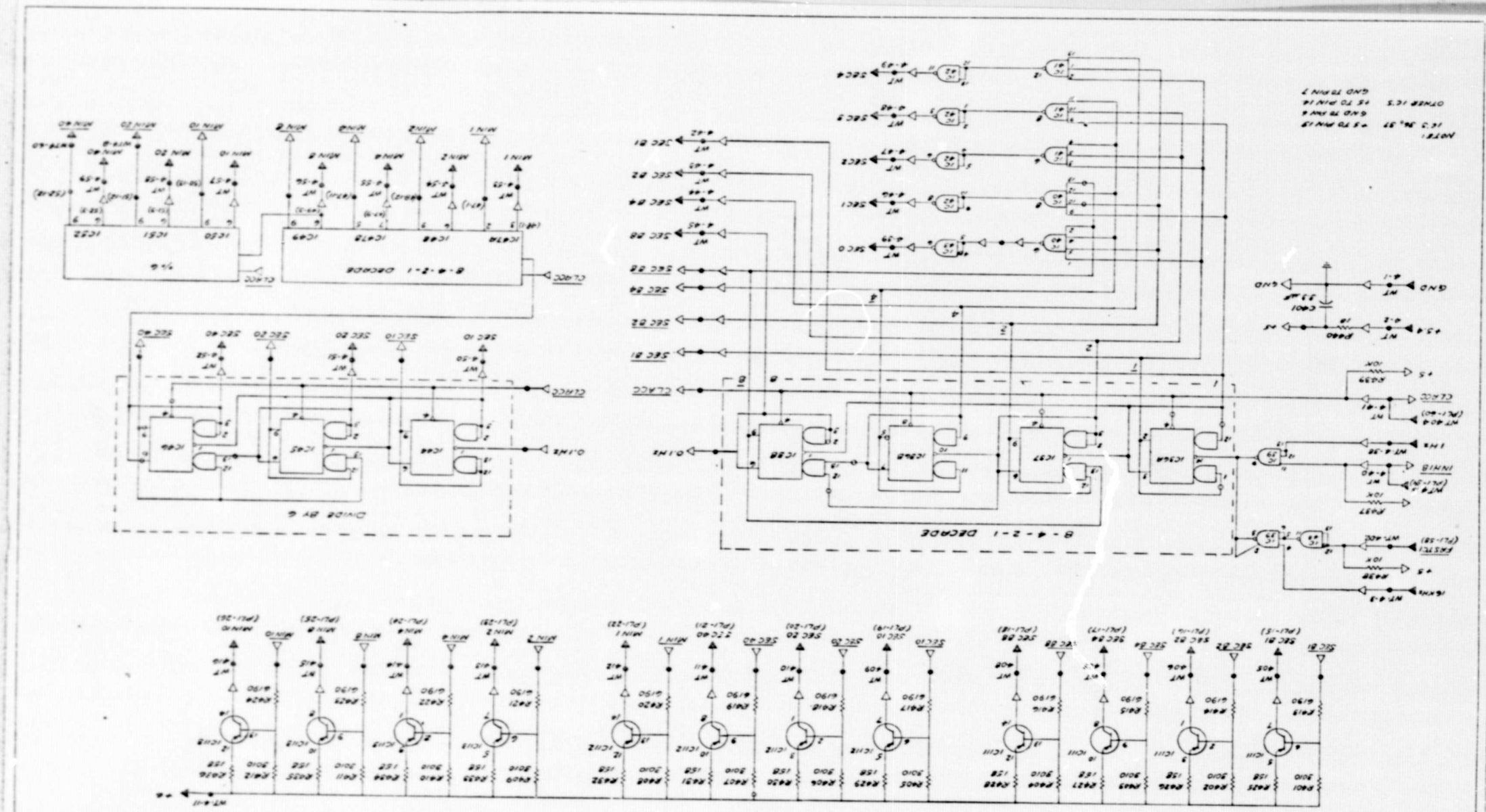
MODULO 10 SHIFT COUNTER

NOTE:
IC 1 +5 CONNECTED TO PIN 4
GND CONNECTED TO PIN 10
IC 3,4,5,6,8,12,13,,108,108 +5 CONNECTED TO PIN 13
GND CONNECTED TO PIN 6
ALL OTHER IC'S +5 TO PIN 14
GND TO PIN 8

NOTE:
IC 16, 17, 23 +5 TO PIN 16
GND TO PIN 8
OTHER IC'S AS TO PIN 14
AND TO PIN 7

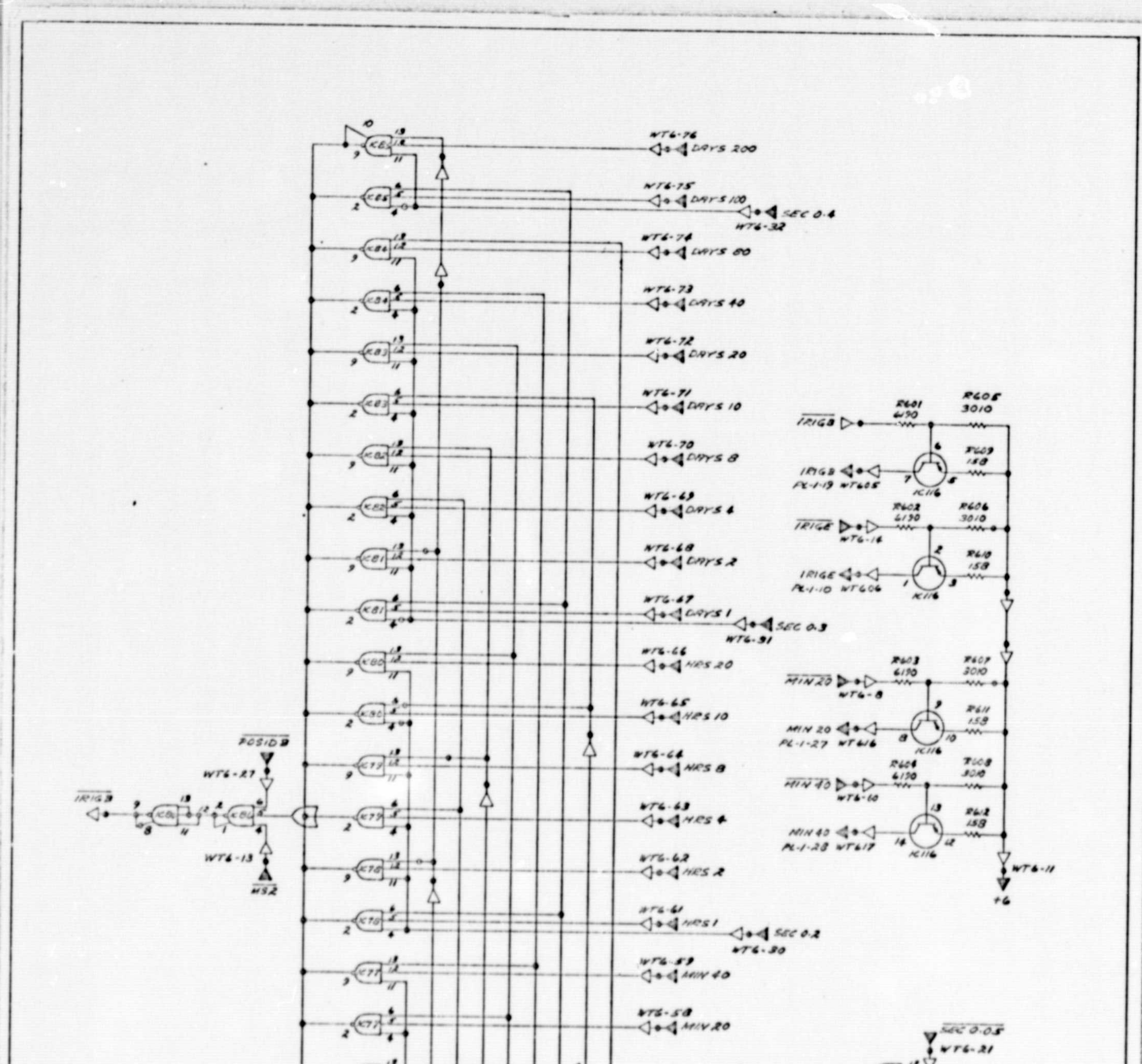
CLOCK CIRCUIT 3

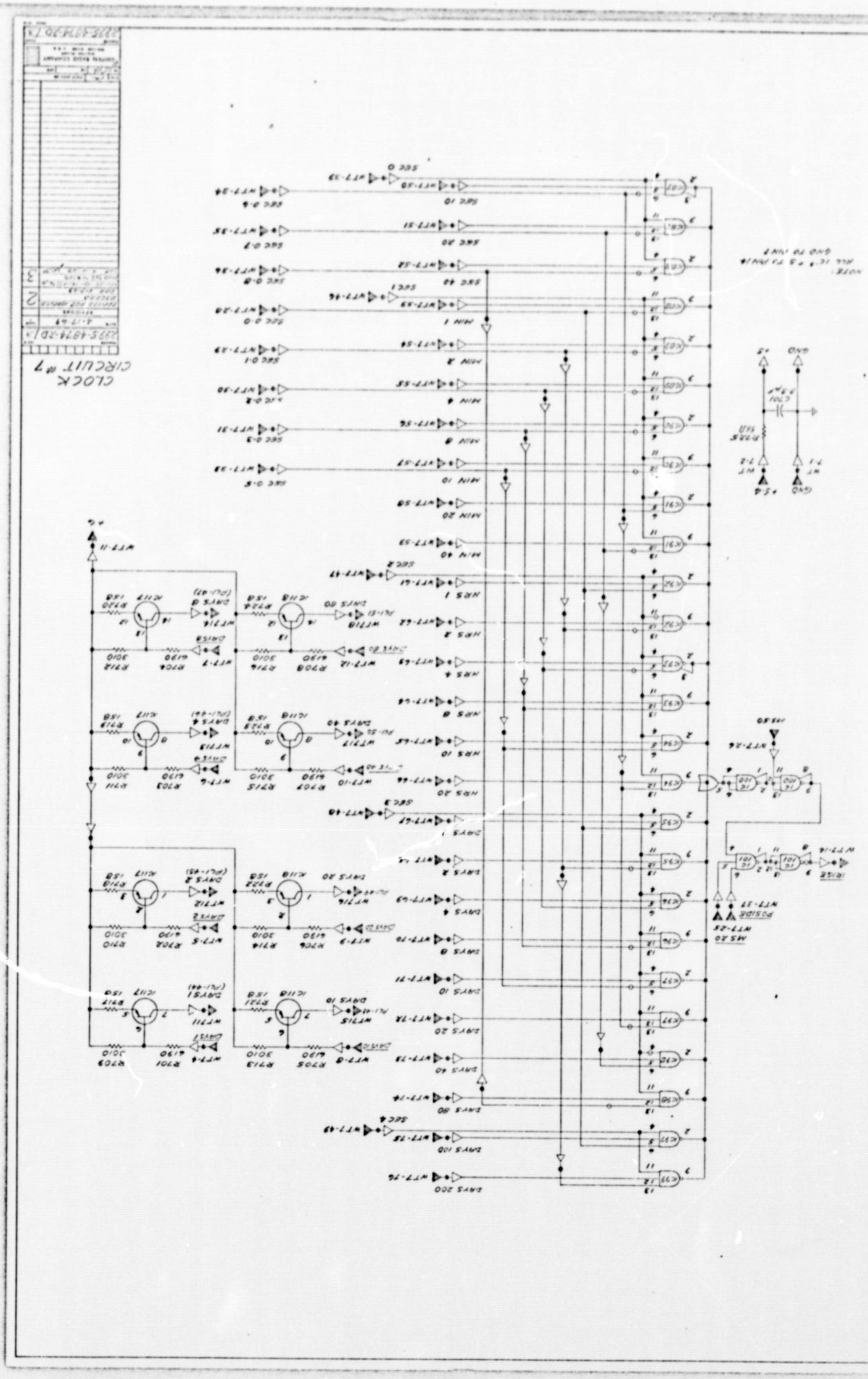



CLOCK CIRCUIT-4
8-4-2-1 DECODE
DIVIDE BY 6
CLKCC
0.1MHz
SEC 0
SEC 1
SEC 2
SEC 4
SEC 8
SEC 10
SEC 20
SEC 40
SEC 80
1MHz
10MHz
100MHz
1KHz
10KHz
100KHz
GND
+5
+12
-12
NOTE:
IC'S 34, 37 +5 TO PIN 14
GND TO PIN 4
OTHER IC'S +5 TO PIN 14
GND TO PIN 7

NOTE:
IC'S 39, 42, 63 +5 CONNECTED TO PIN 14
GND TO PIN 6
ALL OTHER IC'S -5 TO PIN 14
GND TO PIN 7

CLOCK CIRCUIT-5


CLOCK CIRCUIT #6
NOTE:
ALL IC'S +5 TO PIN 14
GND TO PIN 7
IRIG B
POSID B
HSZ
WT6-27
WT6-13
DAYS 200
DAYS 100
DAYS 80
DAYS 40
DAYS 20
DAYS 10
DAYS 8
DAYS 4
DAYS 2
DAYS 1
HRS 20
HRS 10
HRS 8
HRS 4
HRS 2
HRS 1
MIN 40
MIN 20
MIN 10
MIN 8
MIN 4
MIN 2
MIN 1
SEC 40
SEC 20
SEC 10
SEC 8
SEC 4
SEC 2
SEC 1
SEC 0.4
SEC 0.3
SEC 0.2
SEC 0.1
SEC 0.0
SEC 0.00
SEC 0.08
SEC 0.07
SEC 0.06
SEC 0.05
SEC 0.04
SEC 0.03
SEC 0.02
SEC 0.01
IRIG B
IRIG E
MIN 20
MIN 40
R601 6190
R602 6190
R603 6190
R604 6190
R605 3010
R606 3010
R607 3010
R608 3010
R609 158
R610 158
R611 158
R612 158
R613 39
C601 3.3uf
IC116
GND
+5
+5.4
WT6-1
WT6-2
WT6-11
+6


CLOCK
CIRCUIT #7
SEC 0
SEC 10
SEC 20
SEC 40
SEC 1
MIN 1
MIN 2
MIN 4
MIN 8
MIN 10
MIN 20
MIN 40
SEC 2
HRS 1
HRS 2
HRS 4
HRS 8
HRS 10
HRS 20
SEC 3
DAYS 1
DAYS 2
DAYS 4
DAYS 8
DAYS 10
DAYS 20
DAYS 40
SEC 4
DAYS 80
DAYS 100
DAYS 200
MS 10
MS 20
MS 40
MS 80
POSIDE
RISE
GND
+5
NOTE:
ALL IC'S TO MM74
GND TO PIN 7

3: MECHANICAL DESIGN AND PACKAGING

3.1 Introduction

In addition to developing a design of the Engineering Models capable of meeting the environmental requirements for Manned Space Flight, additional packaging goals were set for Part II of the contract. These were reduced size and weight. The construction methods to achieve, and in fact exceed, most of these goals, are discuseed in the balance of this section.

3.2 Outer Case Assembly

The outer case of the SATS is a built-up assembly fabricated from 6061 Aluminum and dip-brazed. This construction technique provides high strength with the use of thin sections. The dip-brazing technique further provides air-tight joints at the many metal interfaces. The assembly is heat treated (to T4), selectively nickel plated (for soldering of hermetic connectors), then chromate conversion coated.

3.3 Optical Package Assembly

One end of the SATS case contains the Optical Package which is hermetically sealed. Hermetic covers, manufactured by Parker Seal Company, are held by screws at each end of the optical package. One end cover is visible in the assembled SATS; one is within the compartment containing the electronics modules. These seals use the "Gask-O-Seal" technique familiar in other NASA applications. Leakage is expected to be approximately 23 cubic centimeters per year for the two bulkhead gaskets, and about 10 cubic centimeters a year for the two hermetic connectors between the Optical Package and module compartment. These rates are based on a pressure differential of one atmosphere.

Pressure tests were conducted on the empty Optical Package compartment to 45psig, with no apparent deformation of the side walls. Pressure was applied internally. As finally assembled, further stiffening contributes further to the stiffness of the assembly.

The Optical Package assembly is foamed in place using NOPCO H-402. This foam is used primarily for its low thermal conductivity. The spaces between the cavity and the inner shield, plus those between the oven assembly and the inner shield are filled with Dow Corning "Sylgard" 188 potting resin. This material is a low-durometer shock-absorbing solventless silicone resin. It has low adhesive ability, good damping qualities, and repairability. Physical and electrical characteristics are very stable over the required temperature and humidity range.

Within the Optical Package assembly is the Lamp Oven Assembly, embedded in Emerson and Cuming FPH "Eccofoam." The FPH has higher thermal conductivity but is used for its higher temperature suitability in the lamp assembly over the NOPCO H-402.

3.4 Module Layout and Construction

The final module layout was developed with consideration of the weight and volume goals, intermodule relationships and signal flow.

Each individual module is housed in a thin aluminum dip-brazed can. Each can has stainless steel threaded inserts for later attachment to the SATS case.

After component attachment to the module boards, the modules are hard interwired before individual potting, again using Sylgard 188.

The hard wired array is then installed in the SATS case and final wiring completed. After checkout, the case is level filled to the access door with Sylgard 188, and the side plate attached.

3.5 Individual Module Construction

A typical module contains one or more etched circuit cards with solder terminals at one end. The etched boards are jigged in place prior to the Sylgard fill.

The Power Supply module is designed as one end of the SATS outer case and is installed at the time of the other electronics modules, prior to overall

resin filling of the SATS case.

3.6 External Connections

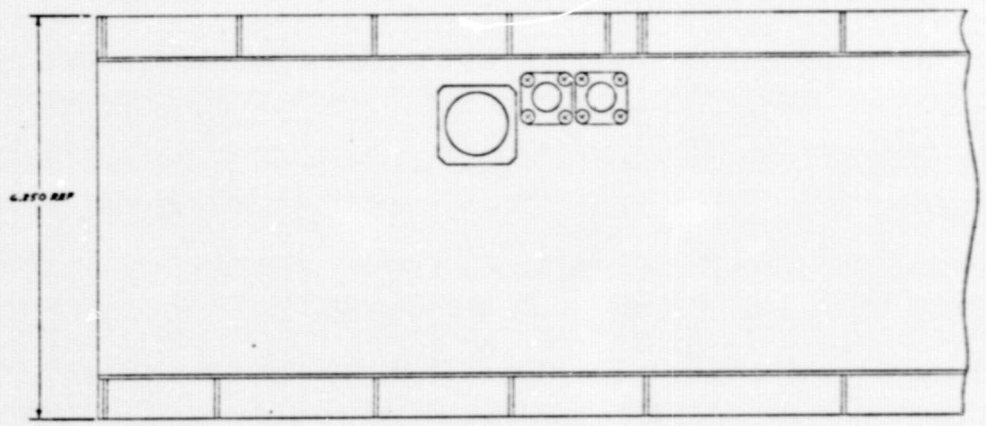
All input and output connections are brought out on the top face of the outer case; this face also carries the identification legends. Factory adjustment holes are present on the top, bottom and sides of the outer case.

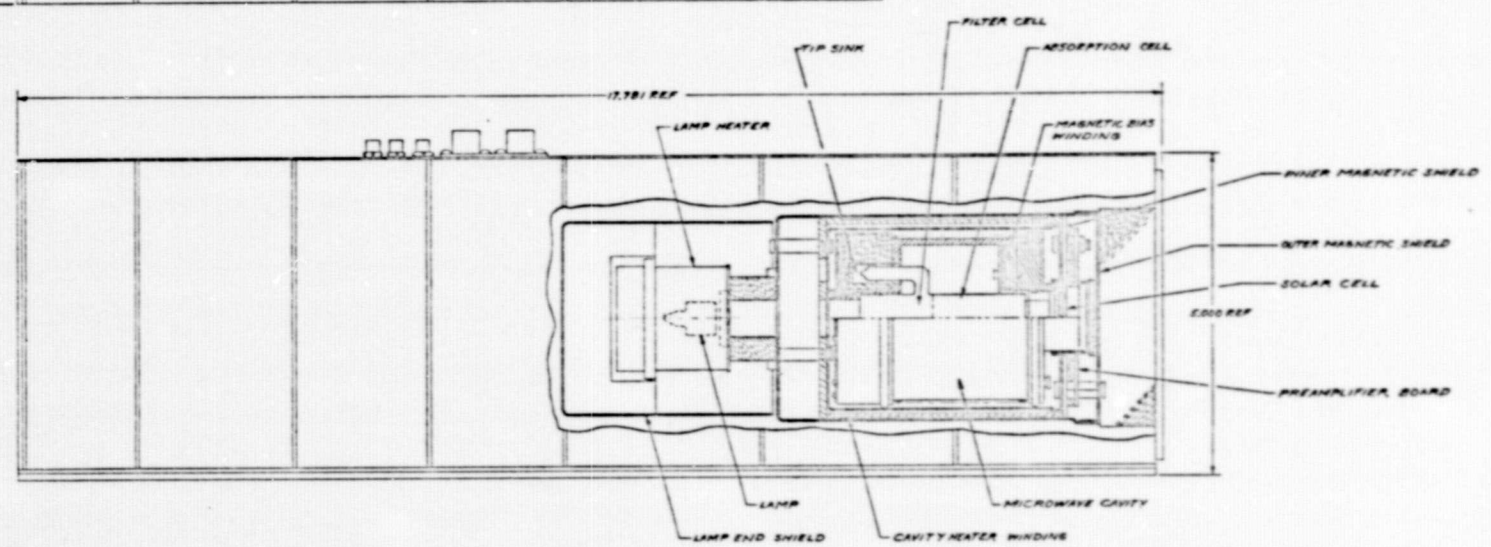
3.7 Mounting of the Complete SATS

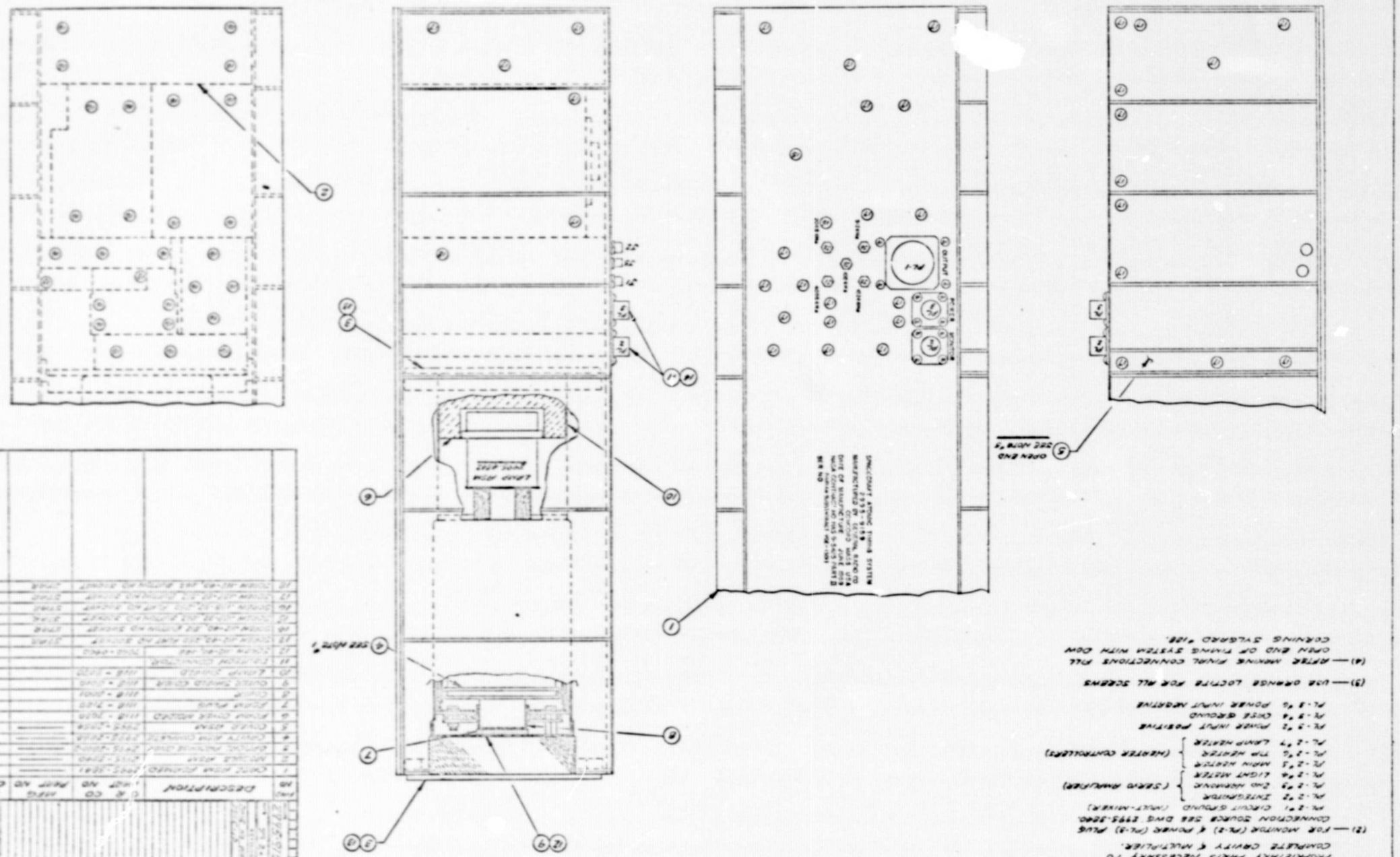
The main SATS case is normally mounted for test and use by 28 screws in the side flanges.

3.8 Attained Mechanical Performance

Work statement goals for weight and volume were 25 lbs and 600 cubic inches, respectively. The final package weighed 18.5 lbs and occupied 441.4 cubic inches, plus mounting flanges. The attained volume including the mounting flanges was 551.8 cubic inches.




FILTER CELL
TIP SINK
ABSORPTION CELL
LAMP HEATER
MAGNETIC BIAS WINDING
INNER MAGNETIC SHIELD
OUTER MAGNETIC SHIELD
SOLAR CELL
PREAMPLIFIER BOARD
LAMP
MICROWAVE CAVITY
LAMP END SHIELD
CAVITY HEATER WINDING



NOTES

(1) — ADM PROCEDURE FOR GENERAL PURPOSE CO MOUNTAINEY PARTS NECESSARY TO COMPLETE CAVITY & MULTIPLIER.

(2) — FOR MONITOR (PL-2) & POWER (PL-3) PLUG CONNECTION SOURCE SEE DWG 5795-3840.

PL-2 #1 CIRCUIT GROUND (MULTI-MIXER)
PL-2 #2 INTEGRATOR
PL-2 #3 2ND HARMONIC (ZERO MULTIPLIER)
PL-2 #4 LIGHT METER
PL-2 #5 MAIN HEATER
PL-2 #6 TM HEATER (HEATER CONTROLLERS)
PL-2 #7 LAMP HEATER
PL-3 #1 POWER INPUT POSITIVE
PL-3 #2 CHEK GROUND
PL-3 #3 POWER INPUT NEGATIVE

(3) — USE OPENED LOCTITE FOR ALL SCREWS

(4) — AFTER MAKING MULTI CONNECTIONS PLACE OPEN END OF TUNING SYSTEM WITH COW CORNING STYCARD #128.

ITEM NO.	DESCRIPTION	C & CO NO.	MFRS NO.	MFG CODE	QTY.
1	CHEST MTG CHASSIS	MT-2881			1
2	CHEST MTG CHASSIS	MT-2882			1
3	CHEST MTG CHASSIS	MT-2883			1
4	CHEST MTG CHASSIS	MT-2884			1
5	CHEST MTG CHASSIS	MT-2885			1
6	CHEST MTG CHASSIS	MT-2886			1
7	CHEST MTG CHASSIS	MT-2887			1
8	CHEST MTG CHASSIS	MT-2888			1
9	CHEST MTG CHASSIS	MT-2889			1
10	CHEST MTG CHASSIS	MT-2890			1
11	CHEST MTG CHASSIS	MT-2891			1
12	CHEST MTG CHASSIS	MT-2892			1
13	CHEST MTG CHASSIS	MT-2893			1
14	CHEST MTG CHASSIS	MT-2894			1
15	CHEST MTG CHASSIS	MT-2895			1
16	CHEST MTG CHASSIS	MT-2896			1
17	CHEST MTG CHASSIS	MT-2897			1
18	CHEST MTG CHASSIS	MT-2898			1
19	CHEST MTG CHASSIS	MT-2899			1
20	CHEST MTG CHASSIS	MT-2900			1
21	CHEST MTG CHASSIS	MT-2901			1
22	CHEST MTG CHASSIS	MT-2902			1
23	CHEST MTG CHASSIS	MT-2903			1
24	CHEST MTG CHASSIS	MT-2904			1
25	CHEST MTG CHASSIS	MT-2905			1
26	CHEST MTG CHASSIS	MT-2906			1
27	CHEST MTG CHASSIS	MT-2907			1
28	CHEST MTG CHASSIS	MT-2908			1
29	CHEST MTG CHASSIS	MT-2909			1
30	CHEST MTG CHASSIS	MT-2910			1
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32	CHEST MTG CHASSIS	MT-2912			1
33	CHEST MTG CHASSIS	MT-2913			1
34	CHEST MTG CHASSIS	MT-2914			1
35	CHEST MTG CHASSIS	MT-2915			1
36	CHEST MTG CHASSIS	MT-2916			1
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38	CHEST MTG CHASSIS	MT-2918			1
39	CHEST MTG CHASSIS	MT-2919			1
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41	CHEST MTG CHASSIS	MT-2921			1
42	CHEST MTG CHASSIS	MT-2922			1
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54	CHEST MTG CHASSIS	MT-2934			1
55	CHEST MTG CHASSIS	MT-2935			1
56	CHEST MTG CHASSIS	MT-2936			1
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58	CHEST MTG CHASSIS	MT-2938			1
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82	CHEST MTG CHASSIS	MT-2962			1
83	CHEST MTG CHASSIS	MT-2963			1
84	CHEST MTG CHASSIS	MT-2964			1
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86	CHEST MTG CHASSIS	MT-2966			1
87	CHEST MTG CHASSIS	MT-2967			1
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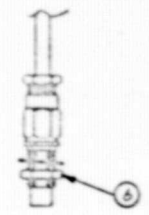
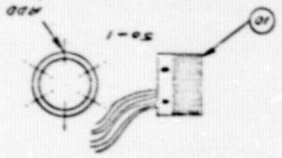
92	CHEST MTG CHASSIS	MT-2972			1
93	CHEST MTG CHASSIS	MT-2973			1
94	CHEST MTG CHASSIS	MT-2974			1
95	CHEST MTG CHASSIS	MT-2975			1
96	CHEST MTG CHASSIS	MT-2976			1
97	CHEST MTG CHASSIS	MT-2977			1
98	CHEST MTG CHASSIS	MT-2978			1
99	CHEST MTG CHASSIS	MT-2979			1
100	CHEST MTG CHASSIS	MT-2980			1

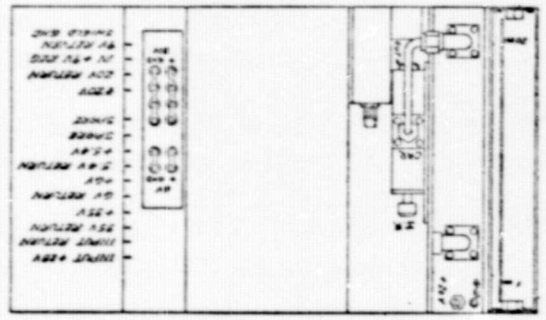
FROM			TO			WIRE		SIGNAL
PLUG	CONNECT PIN	PLUG NO.	CONNECT PIN	PLUG NO.		WIRE COLOR		SIGNAL
J1	1	+20V	10	104-1	A	WH	+20V	+20V
J1	2	OUT	10	104-2	B	WH-GY	20V GROUND	
J1	3	+20V	10	104-3	C	WH	+20V	
J1	4	+20V	10	104-4	D	WH-BK	20V GROUND	
J1	5	+20V	10	104-5	E	WH-BR	MAIN TRANSISTOR	
J1	6	+20V	10	104-6	F	WH-RD	+20V BUS	
J1	7	+20V	10	104-7	G	WH-OR	4-7 20V GND	
J1	8	+20V	10	104-8	H	WH-YL	LOAD THERMISTOR	
J1	9	+20V	10	104-9	J	WH-GN	4-7 20V GND	
J1	10	+20V	10	104-10	K	WH-BL	TH THERMISTOR	
J1	11	+20V	10	104-11	L	WH-VI	TH 20V GND	
J1	12	+20V	10	104-12	M	WH-GY	TH THERMISTOR	
J1	13	+20V	10	104-13	N	WH-WH	4-7 20V GND	
J1	14	+20V	10	104-14	P	WH-BK	4-7 BUS GND	
J1	15	+20V	10	104-15	R	WH-BR	20V GND	
J1	16	+20V	10	104-16	S	WH-RD	+20V BUS	
J1	17	+20V	10	104-17	T	WH-OR	20V GROUND	
J1	18	+20V	10	104-18	U	WH-YL	+20V	
J1	19	+20V	10	104-19	V	WH-GN	20V GROUND	
J1	20	+20V	10	104-20	W	WH-BL	20V GROUND	
J1	21	+20V	10	104-21	X	WH-VI	+20V	
J1	22	+20V	10	104-22	Y	WH-GY	20V GROUND	
J1	23	+20V	10	104-23	Z	WH	+20V	
J1	24	+20V	10	104-24	a	WH	+20V	
J1	25	+20V	10	104-25	b	WH-BK	20V GROUND	
J1	26	+20V	10	104-26	c	WH-BR	MAIN TRANSISTOR	
J1	27	+20V	10	104-27	d	WH-RD	+20V BUS	
J1	28	+20V	10	104-28	e	WH-OR	4-7 20V GND	
J1	29	+20V	10	104-29	f	WH-YL	LOAD THERMISTOR	
J1	30	+20V	10	104-30	h	WH-GN	4-7 20V GND	
J2	1	+20V	1	201-1	A	WH	+20V	
J2	2	OUT	1	201-2	B	WH-GY	20V GROUND	
J2	3	+20V	1	201-3	C	WH	+20V	
J2	4	+20V	1	201-4	D	WH-BK	20V GROUND	
J2	5	+20V	1	201-5	E	WH-BR	MAIN TRANSISTOR	
J2	6	+20V	1	201-6	F	WH-RD	+20V BUS	
J2	7	+20V	1	201-7	G	WH-OR	4-7 20V GND	
J2	8	+20V	1	201-8	H	WH-YL	LOAD THERMISTOR	
J2	9	+20V	1	201-9	J	WH-GN	4-7 20V GND	
J2	10	+20V	1	201-10	K	WH-BL	TH THERMISTOR	
J2	11	+20V	1	201-11	L	WH-VI	TH 20V GND	
J2	12	+20V	1	201-12	M	WH-GY	TH THERMISTOR	
J2	13	+20V	1	201-13	N	WH-WH	4-7 20V GND	
J2	14	+20V	1	201-14	P	WH-BK	4-7 BUS GND	
J2	15	+20V	1	201-15	R	WH-BR	20V GND	
J2	16	+20V	1	201-16	S	WH-RD	+20V BUS	
J2	17	+20V	1	201-17	T	WH-OR	20V GROUND	
J2	18	+20V	1	201-18	U	WH-YL	+20V	
J2	19	+20V	1	201-19	V	WH-GN	20V GROUND	
J2	20	+20V	1	201-20	W	WH-BL	20V GROUND	
J2	21	+20V	1	201-21	X	WH-VI	+20V	
J2	22	+20V	1	201-22	Y	WH-GY	20V GROUND	
J2	23	+20V	1	201-23	Z	WH	+20V	
J2	24	+20V	1	201-24	a	WH	+20V	
J2	25	+20V	1	201-25	b	WH-BK	20V GROUND	
J2	26	+20V	1	201-26	c	WH-BR	MAIN TRANSISTOR	
J2	27	+20V	1	201-27	d	WH-RD	+20V BUS	
J2	28	+20V	1	201-28	e	WH-OR	4-7 20V GND	
J2	29	+20V	1	201-29	f	WH-YL	LOAD THERMISTOR	
J2	30	+20V	1	201-30	h	WH-GN	4-7 20V GND	
J3	1	20V OUT	1	301-1	A	WH-GY	20V GROUND	
J3	2	+20V	1	301-2	B	WH	+20V	
J3	3	OUT	1	301-3	C	WH-BK	20V GROUND	
J3	4	+20V	1	301-4	D	WH-BR	MAIN TRANSISTOR	
J3	5	+20V	1	301-5	E	WH-RD	+20V BUS	
J3	6	+20V	1	301-6	F	WH-OR	4-7 20V GND	
J3	7	+20V	1	301-7	G	WH-YL	LOAD THERMISTOR	
J3	8	+20V	1	301-8	H	WH-GN	4-7 20V GND	
J3	9	+20V	1	301-9	J	WH-BL	TH THERMISTOR	
J3	10	+20V	1	301-10	K	WH-VI	TH 20V GND	
J3	11	+20V	1	301-11	L	WH-GY	TH THERMISTOR	
J3	12	+20V	1	301-12	M	WH-WH	4-7 20V GND	
J3	13	+20V	1	301-13	N	WH-BK	4-7 BUS GND	
J3	14	+20V	1	301-14	P	WH-BR	20V GND	
J3	15	+20V	1	301-15	R	WH-RD	+20V BUS	
J3	16	+20V	1	301-16	S	WH-OR	20V GROUND	
J3	17	+20V	1	301-17	T	WH-YL	+20V	
J3	18	+20V	1	301-18	U	WH-GN	20V GROUND	
J3	19	+20V	1	301-19	V	WH-BL	20V GROUND	
J3	20	+20V	1	301-20	W	WH-VI	+20V	
J3	21	+20V	1	301-21	X	WH-GY	20V GROUND	
J3	22	+20V	1	301-22	Y	WH	+20V	
J3	23	+20V	1	301-23	Z	WH	+20V	
J3	24	+20V	1	301-24	a	WH-BK	20V GROUND	
J3	25	+20V	1	301-25	b	WH-BR	MAIN TRANSISTOR	
J3	26	+20V	1	301-26	c	WH-RD	+20V BUS	
J3	27	+20V	1	301-27	d	WH-OR	4-7 20V GND	
J3	28	+20V	1	301-28	e	WH-YL	LOAD THERMISTOR	
J3	29	+20V	1	301-29	f	WH-GN	4-7 20V GND	
J3	30	+20V	1	301-30	h	WH-BL	TH THERMISTOR	
J4	1	20V OUT	10	104-1	A	WH-GY	20V GROUND	
J4	2	+20V	10	104-2	B	WH	+20V	
J4	3	OUT	10	104-3	C	WH-BK	20V GROUND	
J4	4	+20V	10	104-4	D	WH-BR	MAIN TRANSISTOR	
J4	5	+20V	10	104-5	E	WH-RD	+20V BUS	
J4	6	+20V	10	104-6	F	WH-OR	4-7 20V GND	
J4	7	+20V	10	104-7	G	WH-YL	LOAD THERMISTOR	
J4	8	+20V	10	104-8	H	WH-GN	4-7 20V GND	
J4	9	+20V	10	104-9	J	WH-BL	TH THERMISTOR	
J4	10	+20V	10	104-10	K	WH-VI	TH 20V GND	
J4	11	+20V	10	104-11	L	WH-GY	TH THERMISTOR	
J4	12	+20V	10	104-12	M	WH-WH	4-7 20V GND	
J4	13	+20V	10	104-13	N	WH-BK	4-7 BUS GND	
J4	14	+20V	10	104-14	P	WH-BR	20V GND	
J4	15	+20V	10	104-15	R	WH-RD	+20V BUS	
J4	16	+20V	10	104-16	S	WH-OR	20V GROUND	
J4	17	+20V	10	104-17	T	WH-YL	+20V	
J4	18	+20V	10	104-18	U	WH-GN	20V GROUND	
J4	19	+20V	10	104-19	V	WH-BL	20V GROUND	
J4	20	+20V	10	104-20	W	WH-VI	+20V	
J4	21	+20V	10	104-21	X	WH-GY	20V GROUND	
J4	22	+20V	10	104-22	Y	WH	+20V	
J4	23	+20V	10	104-23	Z	WH	+20V	
J4	24	+20V	10	104-24	a	WH-BK	20V GROUND	
J4	25	+20V	10	104-25	b	WH-BR	MAIN TRANSISTOR	
J4	26	+20V	10	104-26	c	WH-RD	+20V BUS	
J4	27	+20V	10	104-27	d	WH-OR	4-7 20V GND	
J4	28	+20V	10	104-28	e	WH-YL	LOAD THERMISTOR	
J4	29	+20V	10	104-29	f	WH-GN	4-7 20V GND	
J4	30	+20V	10	104-30	h	WH-BL	TH THERMISTOR	
J5	1	+20V	10	104-1	A	WH	+20V	
J5	2	+20V	10	104-2	B	WH-GY	20V GROUND	
J5	3	+20V	10	104-3	C	WH	+20V	
J5	4	+20V	10	104-4	D	WH-BK	20V GROUND	
J5	5	+20V	10	104-5	E	WH-BR	MAIN TRANSISTOR	
J5	6	+20V	10	104-6	F	WH-RD	+20V BUS	
J5	7	+20V	10	104-7	G	WH-OR	4-7 20V GND	
J5	8	+20V	10	104-8	H	WH-YL	LOAD THERMISTOR	
J5	9	+20V	10	104-9	J	WH-GN	4-7 20V GND	
J5	10	+20V	10	104-10	K	WH-BL	TH THERMISTOR	
J5	11	+20V	10	104-11	L	WH-VI	TH 20V GND	
J5	12	+20V	10	104-12	M	WH-GY	TH THERMISTOR	
J5	13	+20V	10	104-13	N	WH-WH	4-7 20V GND	
J5	14	+20V	10	104-14	P	WH-BK	4-7 BUS GND	
J5	15	+20V	10	104-15	R	WH-BR	20V GND	
J5	16	+20V	10	104-16	S	WH-RD	+20V BUS	
J5	17	+20V	10	104-17	T	WH-OR	20V GROUND	
J5	18	+20V	10	104-18	U	WH-YL	+20V	
J5	19	+20V	10	104-19	V	WH-GN	20V GROUND	
J5	20	+20V	10	104-20	W	WH-BL	20V GROUND	
J5	21	+20V	10	104-21	X	WH-VI	+20V	
J5	22	+20V	10	104-22	Y	WH-GY	20V GROUND	
J5	23	+20V	10	104-23	Z	WH	+20V	
J5	24	+20V	10	104-24	a	WH-BK	20V GROUND	
J5	25	+20V	10	104-25	b	WH-BR	MAIN TRANSISTOR	
J5	26	+20V	10	104-26	c	WH-RD	+20V BUS	
J5	27	+20V	10	104-27	d	WH-OR	4-7 20V GND	
J5	28	+20V	10	104-28	e	WH-YL	LOAD THERMISTOR	
J5	29	+20V	10	104-29	f	WH-GN	4-7 20V GND	
J5	30	+20V	10	104-30	h	WH-BL	TH THERMISTOR	
J6	1	20V OUT	10	104-1	A	WH-GY	20V GROUND	
J6	2	+20V	10	104-2	B	WH	+20V	
J6	3	OUT	10	104-3	C	WH-BK	20V GROUND	
J6	4	+20V	10	104-4	D	WH-BR	MAIN TRANSISTOR	
J6	5	+20V	10	104-5	E	WH-RD	+20V BUS	
J6	6	+20V	10	104-6	F	WH-OR	4-7 20V GND	
J6	7	+20V	10	104-7	G	WH-YL	LOAD THERMISTOR	
J6	8	+20V	10	104-8	H	WH-GN	4-7 20V GND	
J6	9	+20V	10	104-9	J	WH-BL	TH THERMISTOR	
J6	10	+20V	10	104-10	K	WH-VI	TH 20V GND	
J6	11	+20V	10	104-11	L	WH-GY	TH THERMISTOR	
J6	12	+20V	10	104-12	M	WH-WH	4-7 20V GND	
J6	13	+20V	10	104-13	N	WH-BK	4-7 BUS GND	
J6	14	+20V	10	104-14	P	WH-BR	20V GND	
J6	15	+20V	10	104-15	R	WH-RD	+20V BUS	
J6	16	+20V	10	104-16	S	WH-OR	20V GROUND	
J6	17	+20V	10	104-17	T	WH-YL	+20V	
J6	18	+20V	10	104-18	U	WH-GN	20V GROUND	
J6	19	+20V	10	104-19	V	WH-BL	20V GROUND	
J6	20	+20V	10	104-20	W	WH-VI	+20V	
J6	21	+20V	10	104-21	X	WH-GY	20V GROUND	
J6	22	+20V	10	104-22	Y	WH	+20V	
J6	23	+20V	10	104-23	Z	WH	+20V	
J6	24	+20V	10	104-24	a	WH-BK	20V GROUND	
J6	25	+20V	10	104-25	b	WH-BR	MAIN TRANSISTOR	
J6	26	+20V	10	104-26	c	WH-RD	+20V BUS	
J6	27	+20V	10	104-27	d	WH-OR	4-7 20V GND	
J6	28	+20V	10	104-28	e	WH-YL	LOAD THERMISTOR	
J6	29	+20V	10	104-29	f	WH-GN	4-7 20V GND	
J6	30	+20V	10	104-30	h	WH-BL	TH THERMISTOR	
J7	1	+20V	1	701-1	A	WH	+20V	
J7	2	+20V	1	701-2	B	WH-GY	20V GROUND	
J7	3	+20V	1	701-3	C	WH	+20V	
J7	4	+20V	1	701-4	D	WH-BK	20V GROUND	
J7	5	+20V	1	701-5	E	WH-BR	MAIN TRANSISTOR	
J7	6	+20V	1	701-6	F	WH-RD	+20V BUS	
J7	7	+20V	1	701-7	G	WH-OR	4-7 20V GND	
J7	8	+20V	1	701-8	H	WH-YL	LOAD THERMISTOR	
J7	9	+20V	1	701-9	J	WH-GN	4-7 20V GND	
J7	10	+20V	1	701-10	K	WH-BL	TH THERMISTOR	
J7	11	+20V	1	701-11	L	WH-VI	TH 20V GND	
J7	12	+20V	1	701-12	M	WH-GY	TH THERMISTOR	
J7	13	+20V	1	701-13	N	WH-WH	4-7 20V GND	
J7	14	+20V	1	701-14	P	WH-BK	4-7 BUS GND	
J7	15	+20V	1	701-15	R	WH-BR	20V GND	
J7	16	+20V	1	701-16	S	WH-RD	+20V BUS	
J7	17	+20V	1	701-17	T	WH-OR	20V GROUND	
J7	18	+20V	1	701-18	U	WH-YL	+20V	
J7	19	+20V	1	701-19	V	WH-GN	20V GROUND	
J7	20	+20V	1	701-20	W	WH-BL	20V GROUND	
J7	21	+20V	1	701-21	X	WH-VI	+20V	
J7	22	+20V	1	701-22	Y	WH-GY	20V GROUND	
J7	23	+20V	1	701-23	Z	WH	+20V	
J7	24	+20V	1	701-24	a	WH-BK	20V GROUND	
J7	25	+20V	1	701-25	b	WH-BR	MAIN TRANSISTOR	
J7	26	+20V	1	701-26	c	WH-RD	+20V BUS	
J7	27	+20V	1	701-27	d	WH-OR	4-7 20V GND	
J7	28	+20V	1	701-28	e	WH-YL	LOAD THERMISTOR	
J7	29	+20V	1	701-29	f	WH-GN	4-7 20V GND	
J7	30	+20V	1	701-30	h	WH-BL	TH THERMISTOR	

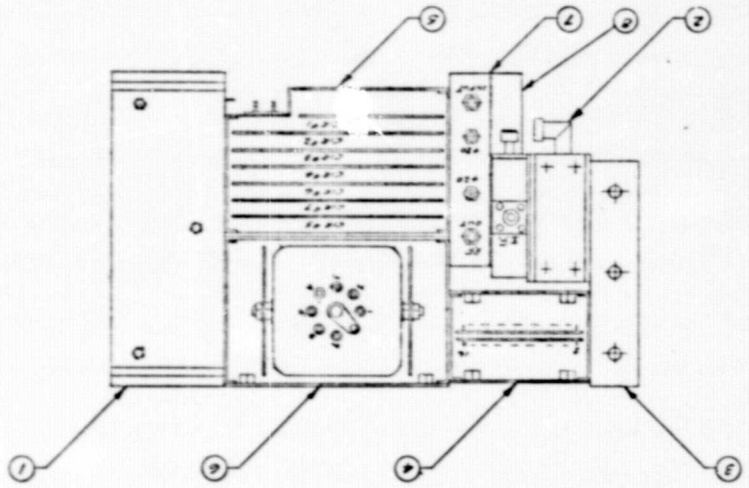
TYPICAL CONNECTION FOR J1, 2, 3, 4, 5, 6 FROM CLOCK MODULE



ADD (3) HOLES (CONTROL TO (3) EXISTING HOLES MARKING A TOTAL OF (6) @ 60° APART







ITEM	DESCRIPTION	(3 CO PART NO	VEND PART NO	QUOTE	NO REQ'D
1	POWER SUPPLY	2015-4002	CUSTOM		1
2	MULTIPLEX MUX	2015-4001	CUSTOM PANEL		2
3	MOTOR CONTROLLER	2015-4005			1
4	7SEG DISPLAY	2015-4004			1
5	CLOCK MODULE	2015-4011			1
6	VOICE & PHONE	2015-4003			1
7	RF AMPLIFIER	2015-4007			1
8	MOD. DATA NETWORK	2015-4010			1
9	CONNECTOR	4220-1810			6
10	CONNECTOR PIN				1
11					
12					
13					

4.0 TEST DATA

Typical data are presented to demonstrate the performance of the SATS designed under Part II of this contract.

4.1 FREQUENCY VERSUS CASE TEMPERATURE

Figure 4.1 shows the temperature dependence of the frequency of the SATS. Frequency was determined by averaging 10 consecutive 100-second measurements. A Cesium Beam Standard was the reference. The error limits shown indicate the reproducibility limits of the measurement. For this measurement, the SATS was placed inside a test chamber with fast air circulation in a normal operating position. No heat sink was used and the case temperature, measured by a thermocouple attached to the mounting flange, was only about 1-2°C higher than the air temperature.

The total frequency change from -35°C to +61°C case temperature is less than 7×10^{-11}, taking the worst case error limits.

4.2 FREQUENCY VERSUS SUPPLY VOLTAGE

Figure 4.2 shows the effect on the SATS frequency when the input voltage is varied. Each point shown was the average of 10 consecutive 10-second reading. The reference was a Cesium Beam Standard. Error limits are indicated. While the graph drawn shows a small frequency change over the input voltage range, its significance is questionable as a straight line could be drawn within the error limits of each point. The worst case indicates about 4×10^{-11} for input voltages from 22 to 34 volts.

4.3 SHORT-TERM STABILITY VERSUS TEMPERATURE

For the measurement of short-term stability with 1-second averaging time the Cesium Beam Standard was replaced by a 5 MHz, precision crystal

oscillator (General Radio 1115-BX) as the 1-second stability of the Cesium Beam Standard is not satisfactory. No significant variation of short-term stability is observed over the full temperature range.

4.4 SHORT-TERM STABILITY (MISCELLANEOUS DATA)

Figure 4.4.1 shows the results of measurements of frequency deviation for averaging times from 0.1 second to 10 seconds. The reference standard is a 5 MHz, precision, crystal oscillator (General Radio 1115-BX). For these measurements the digital circuitry of the SATS was disabled to measure the performance of the rubidium frequency standard part of the SATS. The frequency deviation is:

5.8×10^{-11} rms for $\tau =$ 0.1 second
1.7×10^{-11} rms for $\tau =$ 1 second
5.4×10^{-12} rms for $\tau =$ 10 seconds

These data are consistent with a $\frac{1}{\sqrt{\tau}}$ behavior, predicted by the theory of operation. The contributions of the measuring system (including the reference standard) are also shown. Figure 4.4.3 is a block diagram of this system.

Figure 4.4.2 shows the measured frequency deviation at 25°C when all digital circuits in the SATS are active and all outputs are loaded. The results are somewhat worse than without and indicate a small amount of interference from the digital circuitry affecting the performance of the rubidium standard in the SATS. The difference is small enough to be insignificant.

4.5 INPUT POWER VERSUS TEMPERATURE

As a large percentage of the total power consumed by the SATS is used to heat ovens, the total input power varies as a function of ambient temperature. Figure 4.5 shows the input power at 28 volts versus case temperature. The input

power is:

14.4 W at +61°C
19.0 W at +24°C
29.4 W at -34°C

The accuracy of the power measurement is approximately ±1%.

4.6 INPUT POWER VERSUS INPUT VOLTAGE

Figure 4.6 shows that the power supply efficiency is essentially independent of the input voltage, i.e., the input power does not change over the input voltage range from 22 to 34 volts.

4.7 MAGNETIC FIELD EFFECTS

These measurements indicate the effects of magnetic fields on the frequency of the SATS. Due to the nature of the atomic resonance, the frequency is affected only by fields in the axial direction of the Optical Package. A set of large, calibrated Helmholtz coils was used to generate the ambient field. The susceptibility of individual SATS units varies somewhat due to different magnetic bias points of the Optical Packages. As the magnetic bias is used to compensate for manufacturing tolerances of frequency adjustment of the cells, variations are expected. The data shown represent worst case conditions and the worst frequency change between any orientation in the earth's magnetic field is about 2.5×10^{-11}.

4.8 WEIGHT BUDGET

Table 4.8 compares the original weight estimates with the results achieved. Significant differences reflect design changes from the original concept, particularly in the weight of the major piece of hardware, the SATS case, and the additional Modules for the Magnetic Bias Network and the RF Amplifier.

WEIGHT BUDGET NASA SATS

Item	Weight (Pounds)	
	Original Estimate	Actual
POWER SUPPLY (GULTON)	2.5	2.75
SERVO	1.1	.75
MULTIPLIER (RESDEL)	1.0	.8
VCXO + PLOMS	1.2	1.5
HEATER CONTROLLER	1.0	.75
SATS CASE INCLUDING OPTICAL PACKAGE	10.0	8.2
CLOCK	1.5	2.0
MAGNETIC BIAS NETWORK	*	.1
RF AMPLIFIER	*	.2
HARDWARE, CONNECTORS, FINAL RESIN FILL, + CONTINGENCIES	1.7	1.45
TOTAL	20.0	18.5

* NOT INCLUDED IN ORIGINAL DESIGN

TABLE 4.8

4.9 POWER BUDGET

Table 4.9.1 is a power budget for the SATS operating at 25°C ambient temperature. Each of the four supplies is listed separately. The total power of each module is listed as net power. Table 4.9.2 lists heater power at three temperatures. The figures are for power taken from the +35-volt supply and do not include power supply losses. Table 4.9.3 lists the gross input power for the SATS at three temperatures. The same data are shown, as a graph, in Figure 4.5.

POWER BUDGET SATS

ITEM	WATTS AT 25°C 35 VOLTS	20 VOLTS	6 VOLTS	5.4 VOLTS	TOTAL (NET)
VCXO AND PLOMS (1)	--	3.2	--	--	3.2
MULTIPLIER	--	1.4	--	--	1.4
LAMP OSCILLATOR	--	1.1	--	--	1.1
SERVO	--	.5	--	--	.5
PREAMPLIFIER	--	.05	--	--	.05
RF AMPLIFIER	--	.3	--	--	.3
MAGNETIC BIAS NETWORK	--	.1	--	--	.1
HEATER CONTROLLER	--	.6	.15	--	.75
DIGITAL CIRCUITS	--	.05	1.3	1.5	2.85
MAIN HEATER	3.0	--	--	--	3.0
LAMP HEATER	1.6	--	--	--	1.6
TIP HEATER	.4	--	--	--	.4
					15.25 WATTS

With 80% power supply efficiency, the total input is 19 watts.

(1) includes crystal oven heater power

TABLE 4.9.1

POWER BUDGET - SATS HEATERS (WATTS)

	Temperature		
	-35°C	+25°C	+60°C
MAIN HEATER	6.5	3.0	.9
LAMP HEATER	3.2	1.6	.65
TIP HEATER	.9	.4	.09
CRYSTAL OVEN	3.3	1.5	0.5
TOTAL (NET)	13.9	6.5	2.14

Table 4.9.2

SATS POWER VERSUS TEMPERATURE
AT 28-VOLT INPUT (WATTS)

-34°C	+25°C	+61°C
29.4	19.0	14.3

Table 4.9.3

4.10 VIBRATION AND SHOCK

Vibration and shock tests were conducted at Acton Environmental Testing Corporation. Facilities did not permit the measuring of frequency performance during vibration and the test was for survival only. After the tests, no visible damage was noticed and electrical performance was normal. In particular, no permanent change in frequency was observed. Test report is included.

After delivery to MSC, Houston, preliminary vibration tests indicated, essentially, satisfactory performance under sinusoidal vibration but during high level random vibration test the servo loop unlocked. As the random vibration was considered less critical than the sinusoidal vibration, further investigation was indicated.

Preliminary shock tests at MSC, Houston, showed no significant frequency changes due to shock. Some time after the shock test the SATS failed and was returned for correction. When received at General Radio the SATS was operating normally and, due to the intermittent nature of the problem, it was decided to provoke failure by additional vibration exposure.

This approach was successful and the failure was found to be caused by the 8.192 quartz crystal unit used in the Master Crystal Oscillator. The quartz plate was loose inside its vacuum enclosure due to metal fatigue breakage of the mounting straps. It was immediately obvious that a resonance was required to damage the unit. The crystal unit was specified to have no resonance below 2000 Hz and to operate properly at 15 G acceleration levels.

A spare crystal unit was mounted on a shaker and tests conducted. No resonance was observed when the specified swept vibration was applied, but a careful search, manually, showed an extremely narrow resonance of the crystal

supports at about 1500 Hz. This resonance was too high in Q to be excited under the specified frequency-swept vibration. The resonance was only a few hertz wide.

Under random vibration, there was sufficient energy at the critical frequency to excite the resonance, causing excessive frequency modulation before ultimate catastrophic failure of the quartz crystal unit.

Improved quartz crystals were obtained, the Master Crystal Oscillators rebuilt, and vibration tests on the VCXO-PLOM Module showed excellent performance under vibration. At a sinusoidal vibration level of 5 G,the frequency deviation of the output frequency was less than 1×10^{-9} peak to peak except for a very slight resonance at 360 Hz with 2×10^{-9} peak to peak. This performance is substantially better than required and it is expected that the problems during random vibration have been eliminated. Improved performance under sinusoidal vibration is anticipated.

The Optical Package has a resonance at about 400 Hz with a Q of about 10. It is not considered serious in terms of structural integrity and, because it is sufficiently away from the modulation rate of the servo loop, not detrimental to the performance of the SATS. To correct this resonance, major mechanical changes in the Optical Package would be required.

4.11 SUMMARY OF PERFORMANCE

The test data presented indicate that the objectives of the contract have been met in essential details and prove the feasibility of rubidium frequency standards for space applications. In many areas substantial improvements beyond specifications have been achieved, particularly in size, weight, and power consumption. Table 4.11 compares some of the significant specifications with the results obtained.

	Specifications	Actual
Size	600 in^3	442 in^3
Weight	25 lb	18.5 lb
Max Power (25°C)	30 W	19 W
Max Power (-34°C)	42 W	29.5 W
Short-Term Stability	3×10^{-11}	2×10^{-11}
Frequency versus Temperature	1×10^{-10}	0.7×10^{-10}

Table 4.11

SATS I

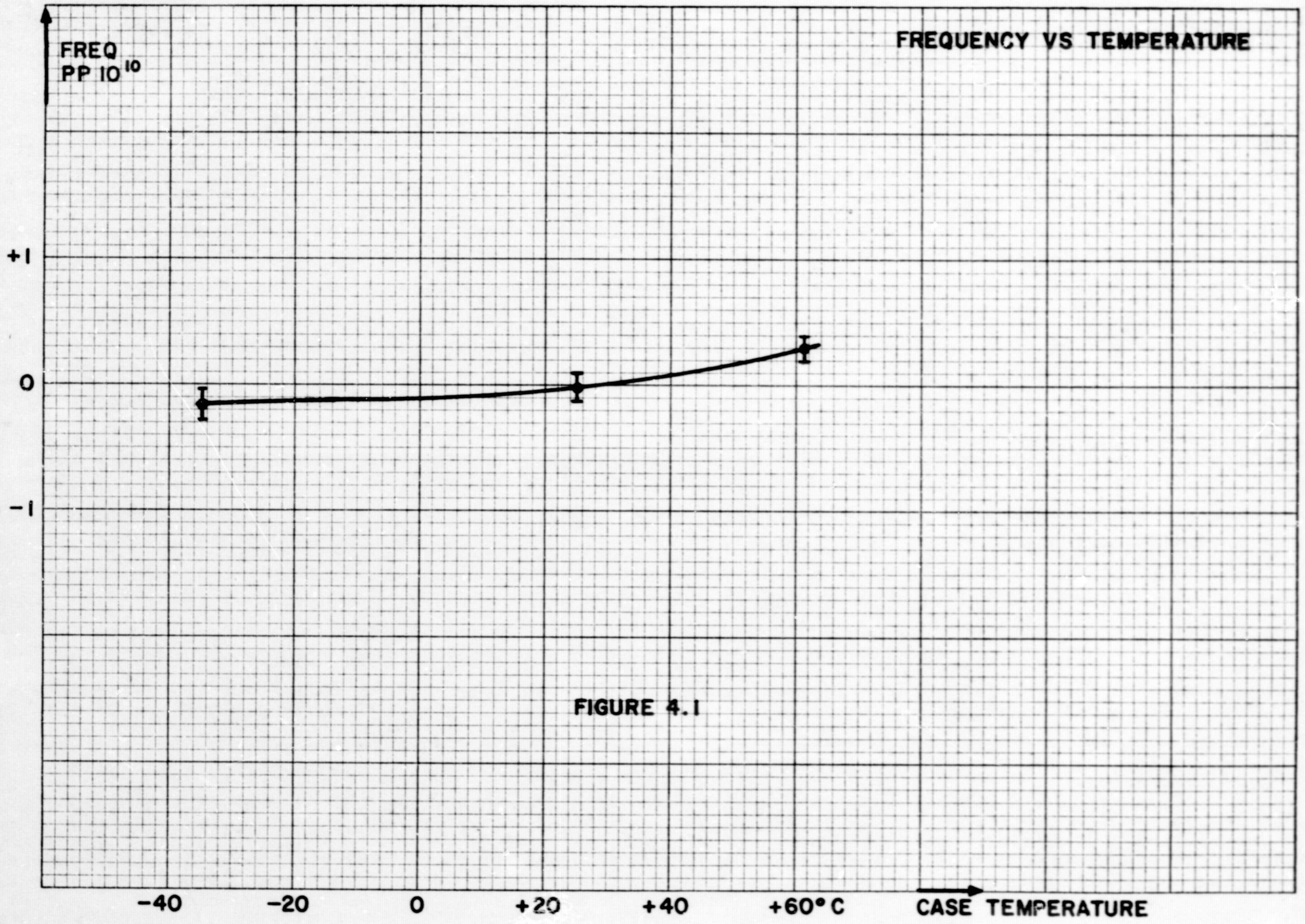


FIGURE 4.1

SATS I

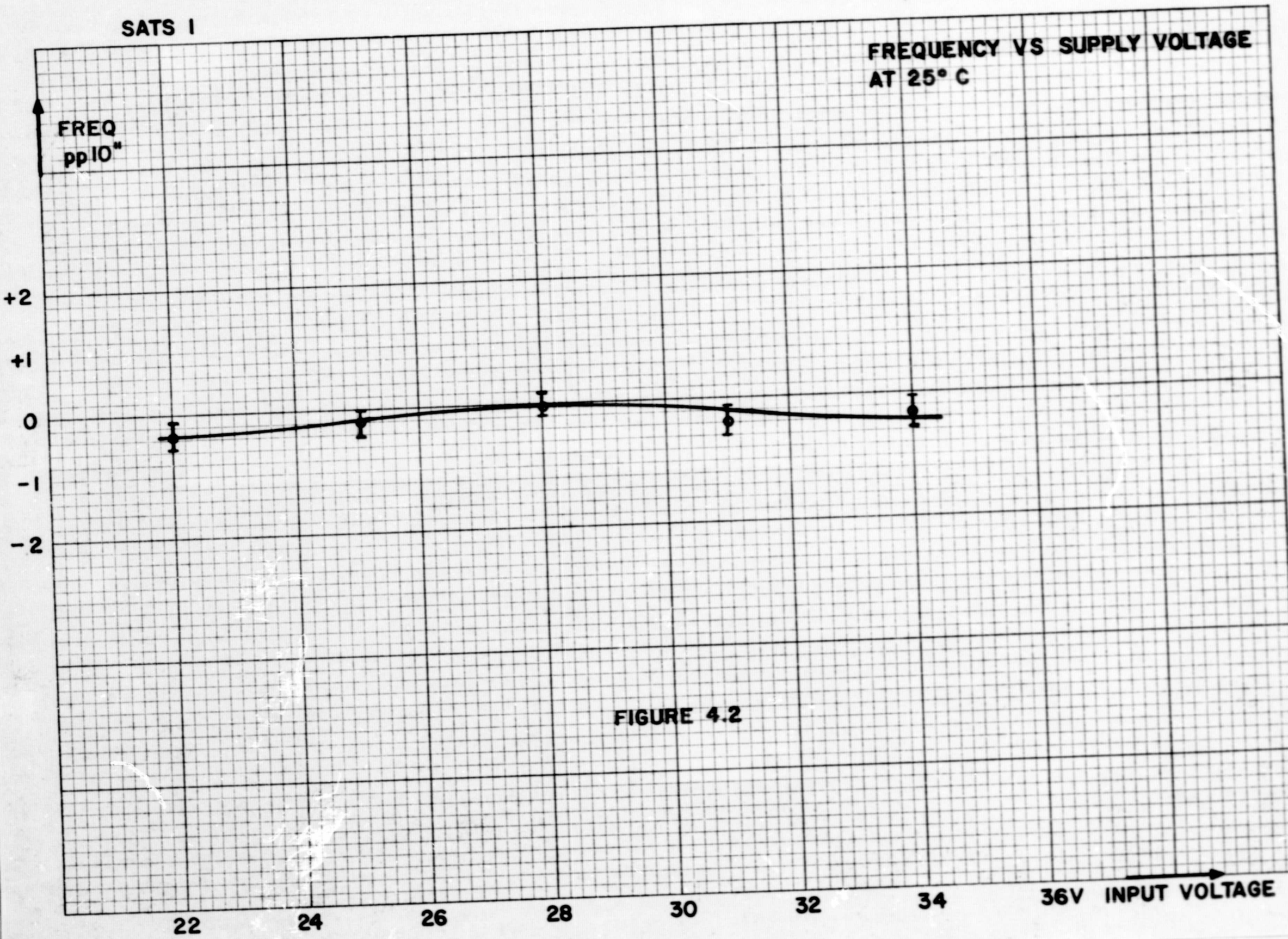


FIGURE 4.2

SATS I

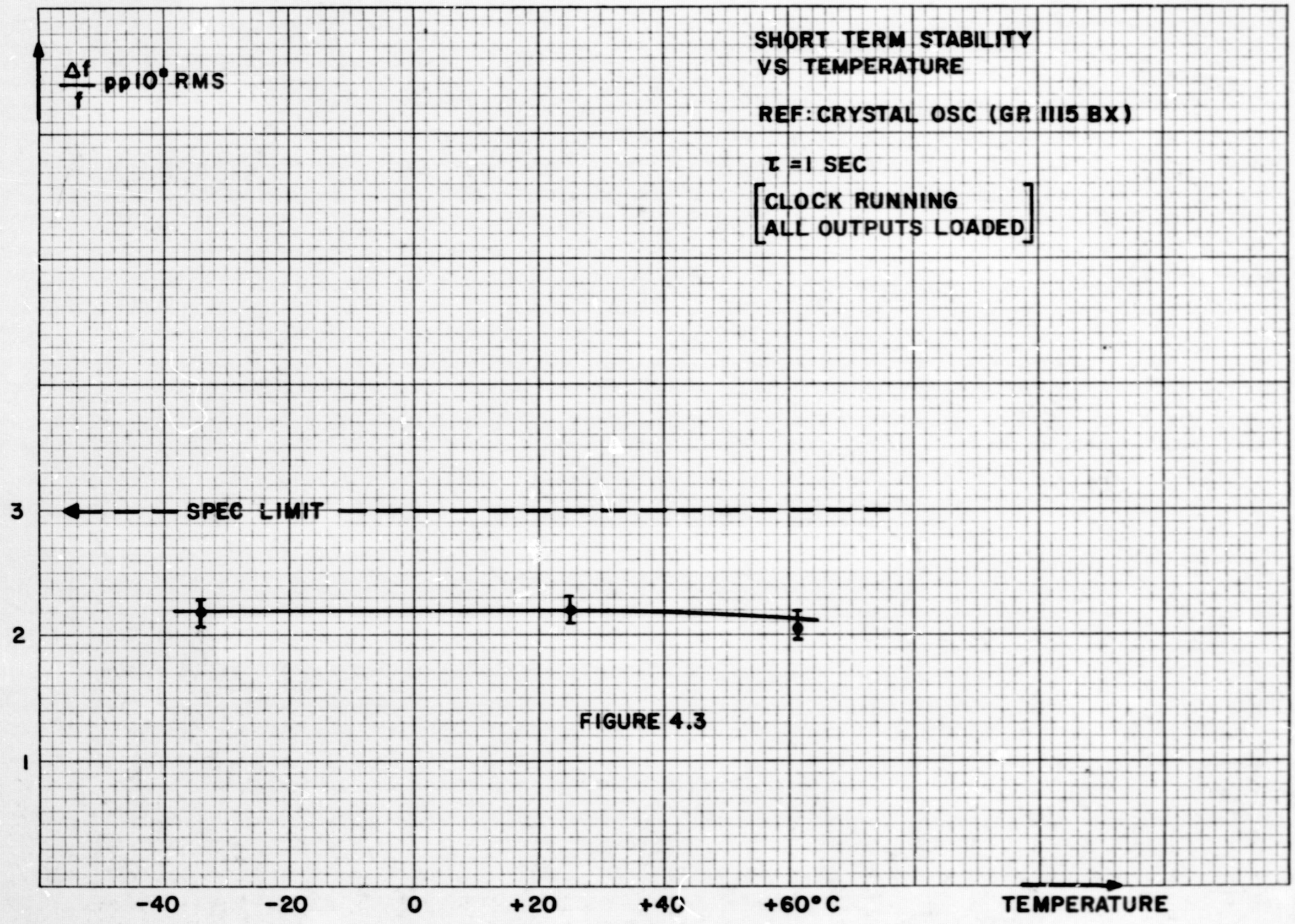


FIGURE 4.3

SATS I

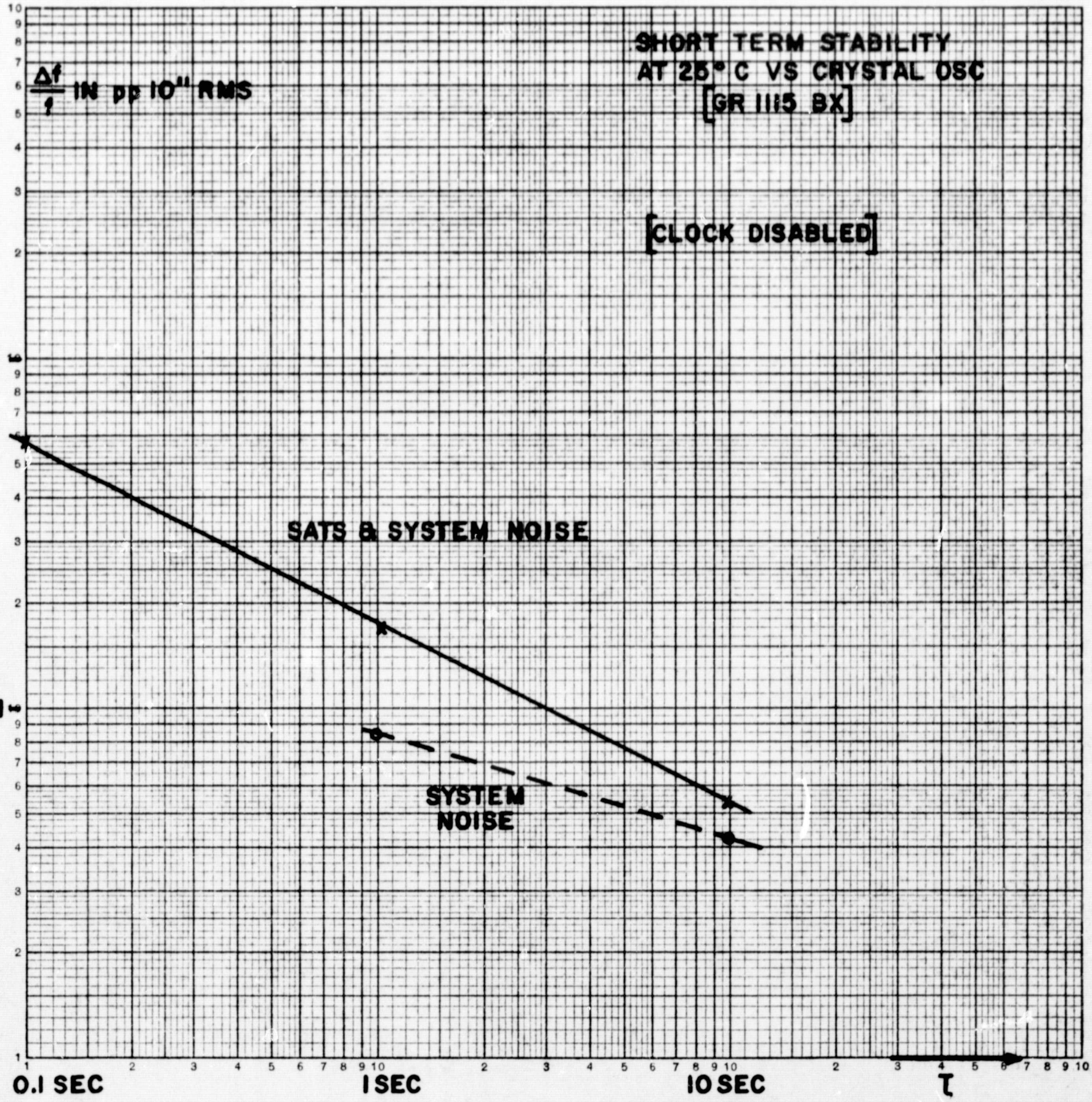


FIGURE 4.4.1

SATS I

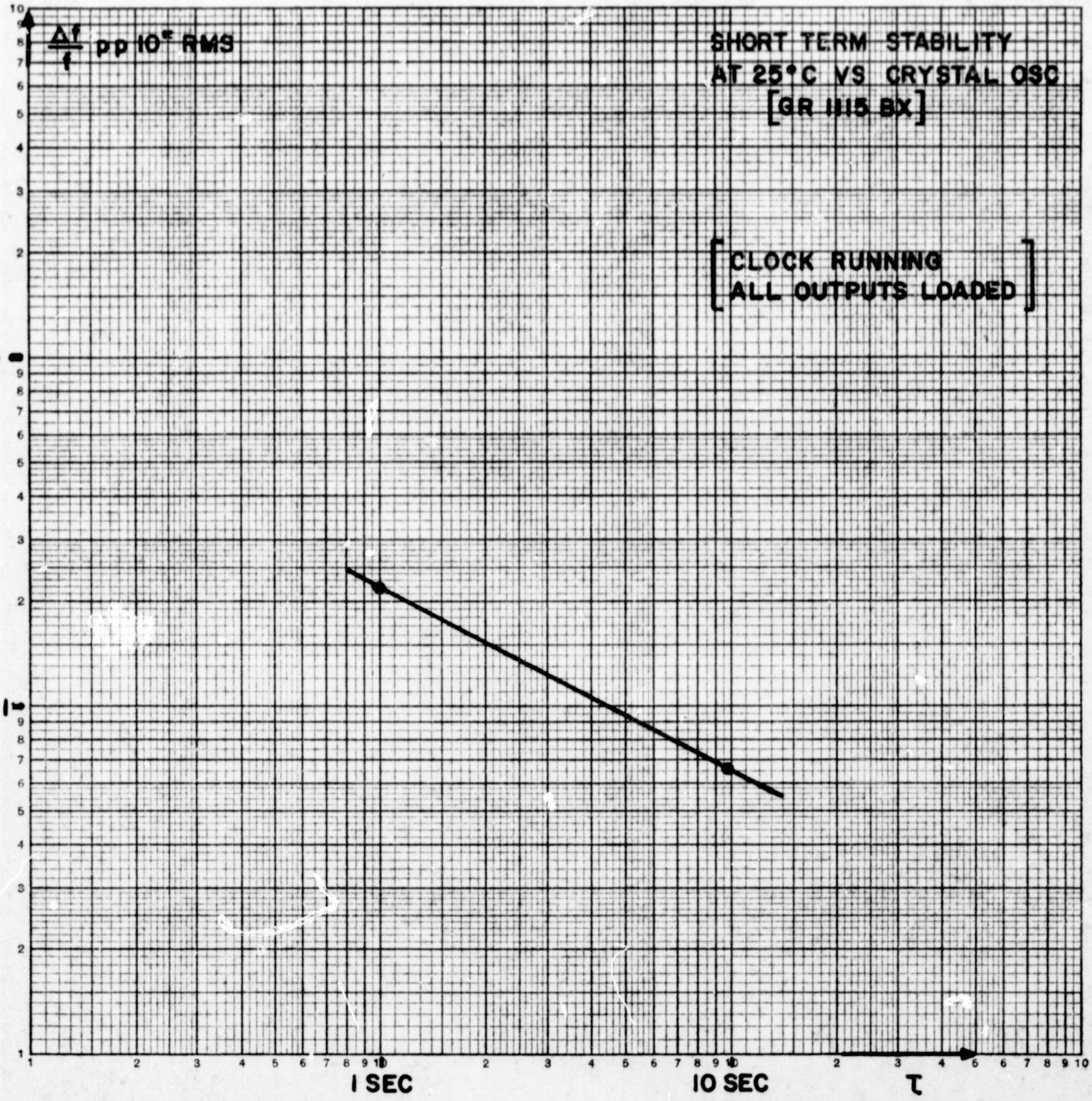
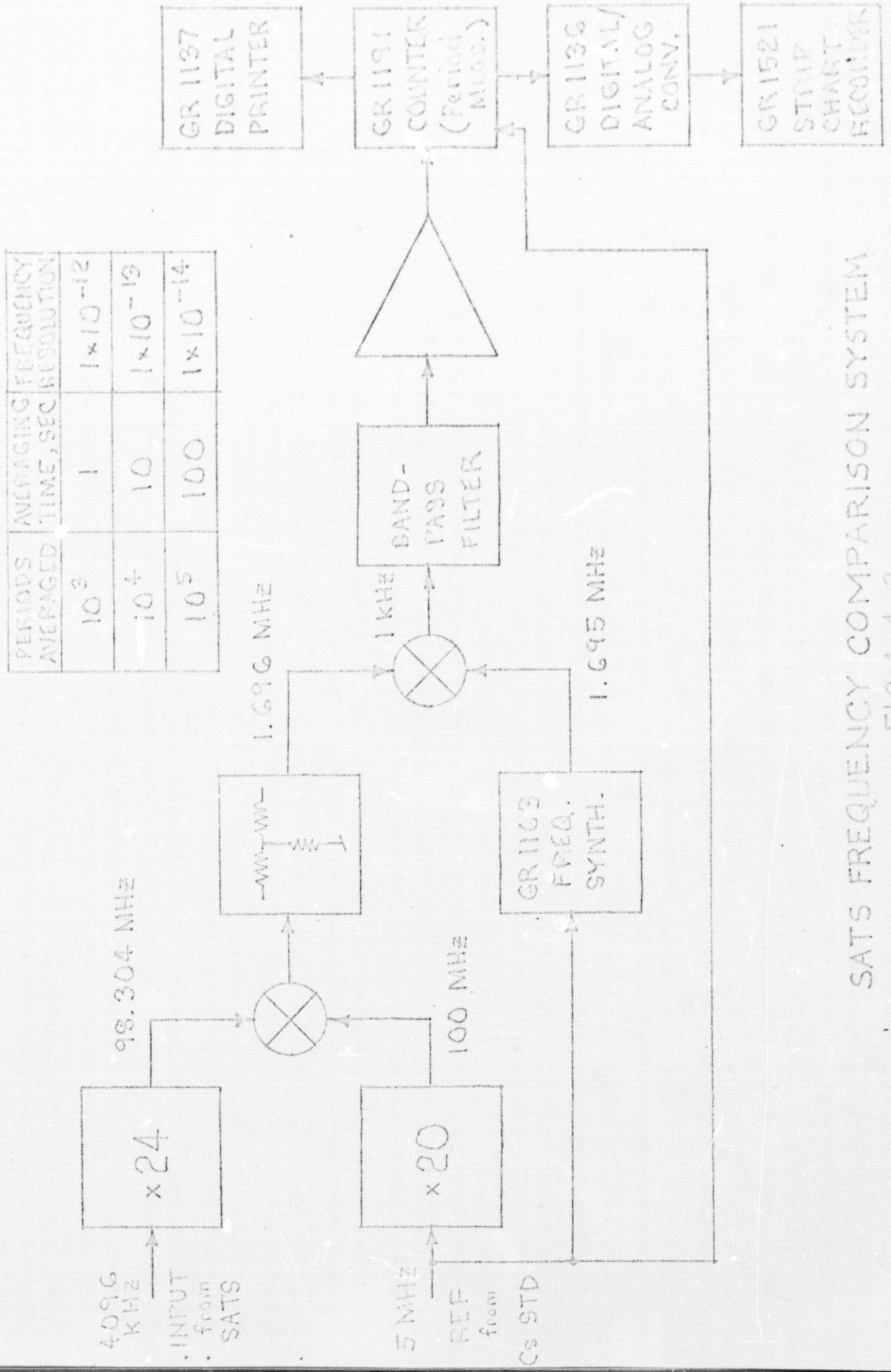


FIGURE 4.4.2



SATS FREQUENCY COMPARISON SYSTEM

FIG 4.4.3

SATS I

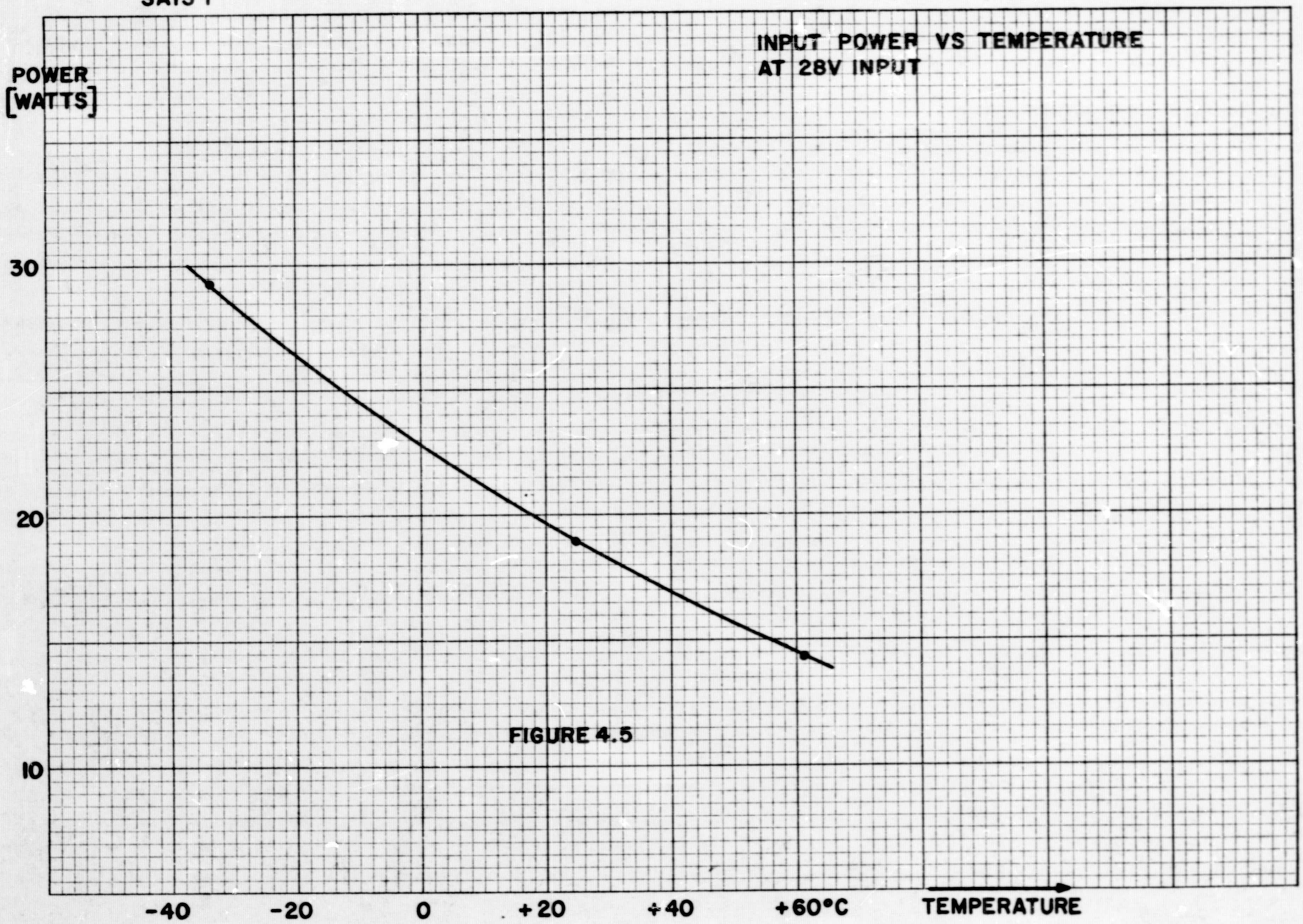


FIGURE 4.5

SATS I

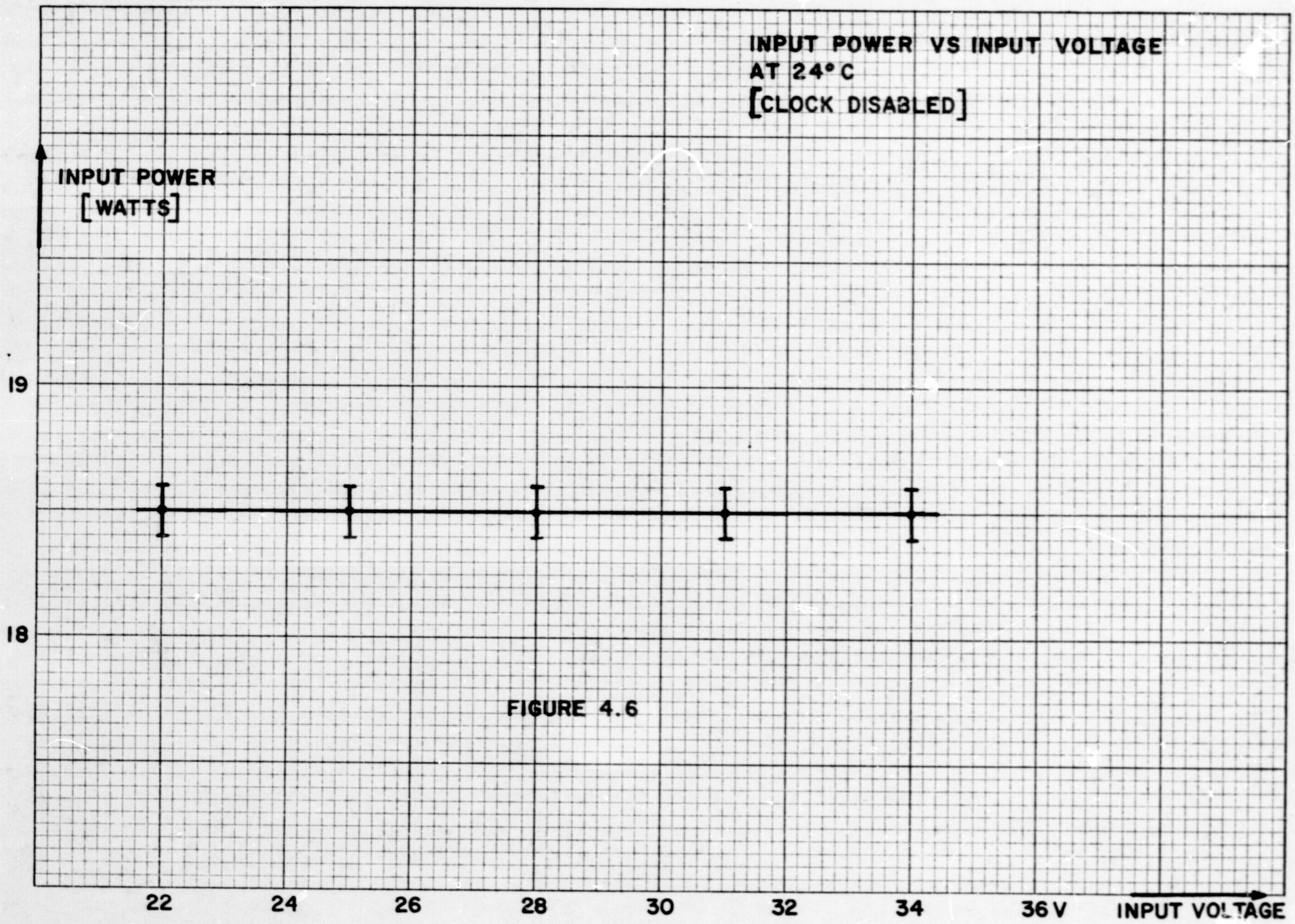


FIGURE 4.6

SATS !

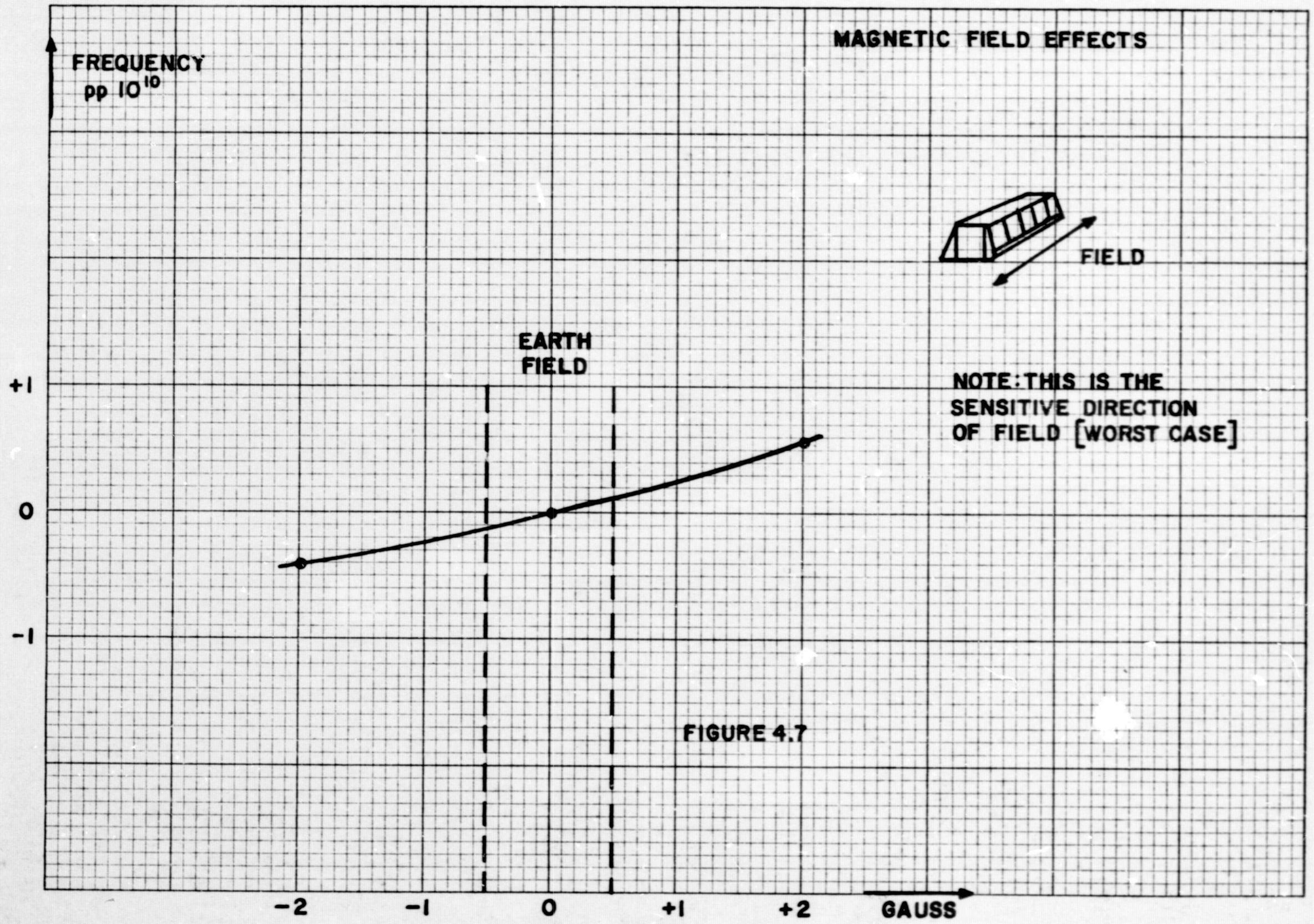


FIGURE 4.7

5 GENERAL DISCUSSION

The basic design of the SATS was carried out under Part I of the contract. Departures from the original design have been made without any significant change of the basic block diagram. Most of the changes have been recommended in the Final Report, Part I, 3.1; others were required to improve the performance to meet the specification for the SATS.

5.1 OPTICAL PACKAGE

The requirements of better thermal performance and short-term stability have been met by substituting an Optical Package of proprietary General Radio design, developed for commercial use. The filter cell and the absorption cell operate at the same temperature, eliminating one complete temperature control system. Combined with a highly efficient light source for optical pumping, this design has improved the short-term st bility (1 second) by 5:1 and the stability over the temperature range by about 7:1. At the same time, lower thermal losses have resulted in a very substantial reduction in power requirement. Total power for the Optical Package was reduced from 26 watts to 15 watts at -34°C. The pressure sensitivity of the absorption cell is such that it was not necessary to reduce the operating pressure of the sealed Optical Package below atmospheric level, reducing the significance of small leakage during long periods of storage.

5.2 POWER SUPPLY

The power supply had to be redesigned to meet the requirements for total dc isolation of the SATS from the input power supply lines. By careful design and elimination of some inefficient (dissipative) regulators, the overall efficiency

was increased from 64% (Part I) to 80% in spite of much increased power going through the converter (all high-powered heaters of the original SATS design took the power from the unregulated input line). Improved stability of the critical 20-volt regulated supply was achieved by using an external precision reference voltage.

5.3 MASTER CRYSTAL OSCILLATOR

A proprietary General Radio design was adopted because of its improved performance, ready availability, and the large amount of performance data on hand due to large volume production.

The choice of a crystal operating at 8.192 MHz rather than 16.384 MHz was made because of the oscillator design and the possibility to eliminate one flip-flop in the synthesizer/multiplier circuits. In addition, this unit contains a precision zener reference diode inside the oven, making available, a very stable reference voltage for the power supply precision regulator.

5.4 14.848-MHz SIGNAL

The original design derived the 14.848-MHz signal by subtracting (in a mixer) 1.536 MHz from 16.384 MHz. The 1.536-MHz signal was obtained by dividing the 16.384 by a factor of 32 to 512 kHz and then multiplying by 3. Temperature dependence of the output as well as the relatively large size of the tuned circuits required have led to the substitution of a simple Phase-Locked Crystal-Oscillator Multiplier (PLCM) which produces the 29th harmonic of the 512 kHz.

5.5 MULTIPLIER CHAIN

In Part I, the High-Frequency Multiplier was driven from 20.480 MHz derived by adding 16.384 MHz and 4.096 MHz. This 20.480-MHz signal was multiplied

X 9 to 184.32 MHz. A step-recovery diode multiplier produced the required signal at 6.8 GHz (X 37). Severe difficulties were encountered and a major redesign was recommended.

The new design starts with a 4.096-MHz signal which is multiplied to 61.44 MHz (X 15) by a Phase-Locked Crystal Oscillator Multiplier (PLOM). A new design for the Microwave Multiplier/Mixer section was subcontracted to Resdel Engineering, Arcadia, California, chosen with approval from Varian and NASA. This unit multiplies the 61.44 MHz to 184.32 (X 3) and then by 37 in a step-recovery diode multiplier. The breadboard unit submitted showed excellent performance in all tests.

The first of the deliverable units was received in May 1969. Test data, while not as good as the breadboard data, indicated satisfactory performance. After complete assembly and potting of the first SATS, this unit failed. The failure occurred at high temperature and was evidenced by a 6:1 reduction in signal amplitude from the Optical Package. Later investigation showed that this was due to parametric oscillations of the step-recovery diode. The unit was removed from SATS and returned to the supplier. As the second unit had not been delivered at that time, no further work could be done on SATS I. It took in excess of four months and three design/rework/evaluation cycles before this problem was solved. In addition, difficulties developed with the mixer unit, obtained by Resdel from Melabs. The original breadboard unit of the Microwave Multiplier/Mixer was returned to Resdel for investigation of any possible differences. Ultimately, the difficulties with the multipliers were resolved by Resdel, but the problems with the Melabs mixer (poor conversion efficiency and erratic performance) were not solved until completely new mixers were obtained from Aertech and the Melabs units abandoned.

The wide range of ambient temperatures specified for the SATS combined with the requirement for stable output level makes the design of this multiplier difficult. It appears that such multipliers can be built. Advances of the state of the art may make this task easier. As the frequency of the SATS is affected by microwave level changes, further improvement of this multiplier would be desirable. Until advanced state of the art makes this practical, an alternate solution should be considered for further development.

Much improved performance over the entire temperature range can be obtained by locating the step-recovery diode with its associated circuitry and the mixer inside the oven in the Optical Package. At constant operating temperature, the step-recovery diode multiplier can easily be adjusted for optimum performance and will not be subject to the difficulties observed. This requires some redesign of the Optical Package to provide room inside the Main Oven, but the overall size of the Optical Package may not have to be changed. Careful investigation would be required to determine other consequences such as: additional heat in the Main Oven and magnetic field due to current through the diode.

5.6 DIGITAL CIRCUITS

Substantial effort was required to improve the clock setting arrangement. The maximum time for updating the clock was reduced from about 6 minutes to less than 1 second. Much longer cables between the SATS and the clock updating control are now permissible. Provisions for programming the clock for 365-day or 366-day (leap year) intervals and short-circuit protected output buffers for the low-frequency digital circuits were designed as required by changes in the specifications for the SATS.

5.7 100-kHz SYNTHESIZER

The original design used analog mixing to add 128 kHz and 16 kHz to 144 kHz. This 144-kHz signal was then added in another mixer to the 256 kHz for 400-kHz output, followed by a 4:1 divider to get 100-kHz output. A total of seven tuned circuits was required for filtering and temperature compensation proved difficult. A digital mixing arrangement was designed to replace the two mixers and the number of tuned circuits reduced to two.

5.8 MISCELLANEOUS

Frequency changes caused by connecting the cables to the Test and Calibration Unit reported in Final Report, Part I, 2.2 have been eliminated. Test cables can now be connected or disconnected without effects on the frequency of the SATS.

6.0 RECOMMENDATIONS AND CONCLUSIONS

Difficulties experienced with the Microwave Multiplier/Mixer over the wide ambient temperature range suggest that, in future development, particular attention to this unit is required. The possibility of locating the Microwave Multiplier/Mixer inside the Main Oven of the Optical Package should be investigated since that approach is likely to eliminate the problems encountered.

The digital circuits should be located in a completely separate compartment to reduce interference on the rubidium reference. While not of significance for the 1-second short-term stability as specified, this interference becomes increasingly more important for any potential applications where shorter averaging times are used.

Better accessibility of test points for factory checkout and calibration is desirable to improve maintainability.

The feasibility of a Spacecraft Atomic Timing System using a hyperfine transition of rubidium as frequency reference has been demonstrated. Significant improvements in the state of the art have been made. Higher operating temperature, wider temperature range, and less size, weight, and power consumption are the most important achievements.

Test Report No. 7123 No. of Pages 14

Report of Test on

NASA SATS
for
GENERAL RADIO COMPANY
under
PURCHASE ORDER NO. 32205-5

ACTON ENVIRONMENTAL TESTING CORPORATION

Date June 25, 1969

	Prepared	Checked	Approved
By	A.LeBourdais	M.Casaubon	M.L.Tolf
Signed	A. LeBourdais	M. Casaubon	M. L. Tolf
Date	6-25-69	6/25/69	6/25/69

Administrative Data

1.0 Purpose of Test: To subject test item to vibration and shock exposure.

2.0 Manufacturer: General Radio Company

3.0 Manufacturer's Type or Model No: NASA SATS

4.0 Drawing, Specification or Exhibit: Development Flight Instrumentation Environmental Type and Flight Spec. IESD Document 19-2, 1 June 1965

5.0 Quantity of Items Tested: One (1), S/N 1.

6.0 Security Classification of Items: Unclassified

7.0 Date Test Completed: June 16, 1969

8.0 Test Conducted By: D. McLaughlin

9.0 Disposition of Specimens: Returned to General Radio Company

10.0 Abstract: No visible or apparent evidence of damage or deterioration to the test item as a result of vibration and shock tests.

1.0 REQUIREMENTS

1.1 VIBRATION

1.1.1 Random and sinusoidal motion shall be applied sequentially along each of three (3) mutually perpendicular axes for a total of 36 minutes. Random spectra is referenced to a log-log plot and held to a ±30% power spectral density.

12.3 g RMS for five (5) minutes

10 Hz .01g^2/Hz

10-75 Hz Linear increase to .14g^2/Hz

75-200 Hz Constant .14g^2/Hz

200-2000 Hz Linear decrease to .05g^2/Hz

5 g RMS for twenty-five (25) minutes

10 Hz .0017g^2/Hz

10-75 Hz Linear increase to .023g^2/Hz

75-200 Hz Constant .023g^2/Hz

200-2000 Hz Linear decrease .0082g^2/Hz

1.1.2 Sinusoidal motion shall be swept logarithmically from 5 Hz to 2 KHz to 5 Hz in 6 minutes in each of the three (3) mutually perpendicular axes.

5 - 10 Hz Constant .20 in D.A.

10-26 Hz Constant ±1g

26-56 Hz Constant .03 in D. A.

56-2000 Hz Constant ±5g

Report No. 7123

1.2 SHOCK

1.2.1 Shock impulses at 30 g's for 11 ±1 milliseconds. There will be three (3) shocks in each direction of three (3) mutually perpendicular axes for a total of 18 shock impulses. Shock input will be a saw-tooth wave form with 10 ±1 milliseconds rise and 1 ±1 milliseconds decay time. Component shall be operating during test.

2.0 PROCEDURES

2.1 VIBRATION

The test item, secured by its normal means to a non-resilient test fixture secured to the exciter of the vibration system, was subjected to the random vibration test per requirements.

Following the vibration test, the test item was visually examined.

2.2 SHOCK

The test item, mounted by its normal means to a non-resilient test fixture secured to the platform of the shock machine, was subjected to the shock test per requirements.

Following the shock test, the test item was visually examined.

3.0 RESULTS

3.1 VIBRATION

There was no visible or apparent evidence of damage or deterioration to the test item as a result of the vibration test.

3.2 SHOCK

There was no visible or apparent evidence of damage or deterioration to the test item as a result of the shock test.

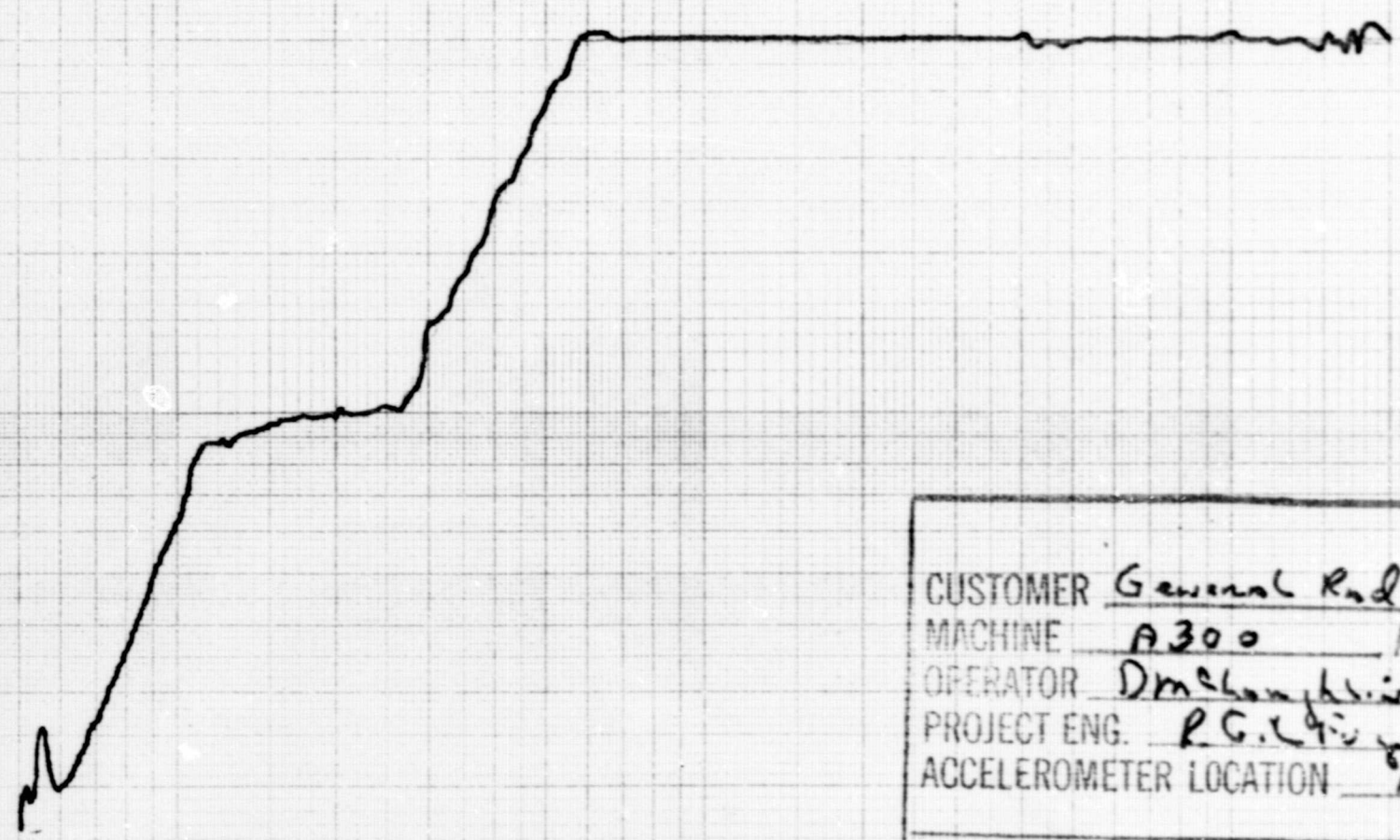
4.0 TEST EQUIPMENT USED

NAME	MFGR.& MODEL	SER.#	RANGE	ACCURACY	INV.#	CAL.FREQ.
Accelerometer	B&K,4335	176854	2Hz-6KHz	±5%		12 Months
Accelerometer	Endevco,2215E	UE56	2Hz-6KHz	±5%		12 Months
Equalizer/Analyzer Auto Random 46-ch	Ling,ASDE40	35	10Hz-2KHz .001-10g^2/Hz	±1DB	PE-315	1 Month
X-Y Recorder	Moseley,135CR	400	.5MV-10V/Div.	±.1%FS	RE-319	3 Months
Log Converter	Moseley,60D	299	60 DB	±.5DB	PE-323	3 Months
Amplifier	Ling,CP10/16VC	41914	5Hz-5KHz	2% Freq.		
Exciter	Ling,A-300	59	6000 lb.force	5% Ampl.	PE-314	1 Month
Shock Machine	AVCO,SM-110		10-5000g	10%	PE-312	With use
Oscilloscope	Tektronix,564	11582	DC-10MCHz	±2%	OS-309	3 Months
Charge Amp.	Kistler,563	895	DC-150KHz	±1MV	AM-316	6 Months

10.0

8.0

1.0

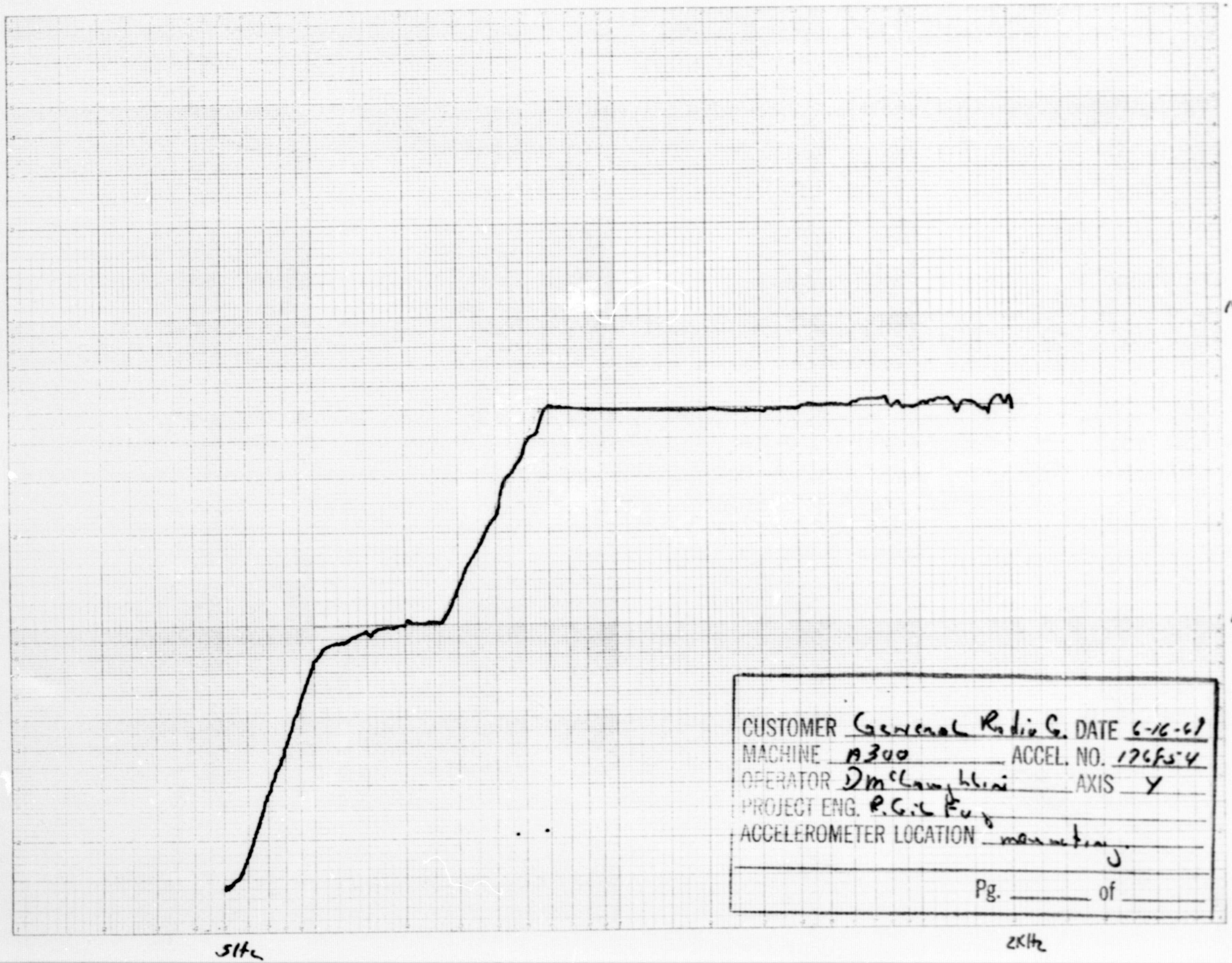


5Hz

2KHz

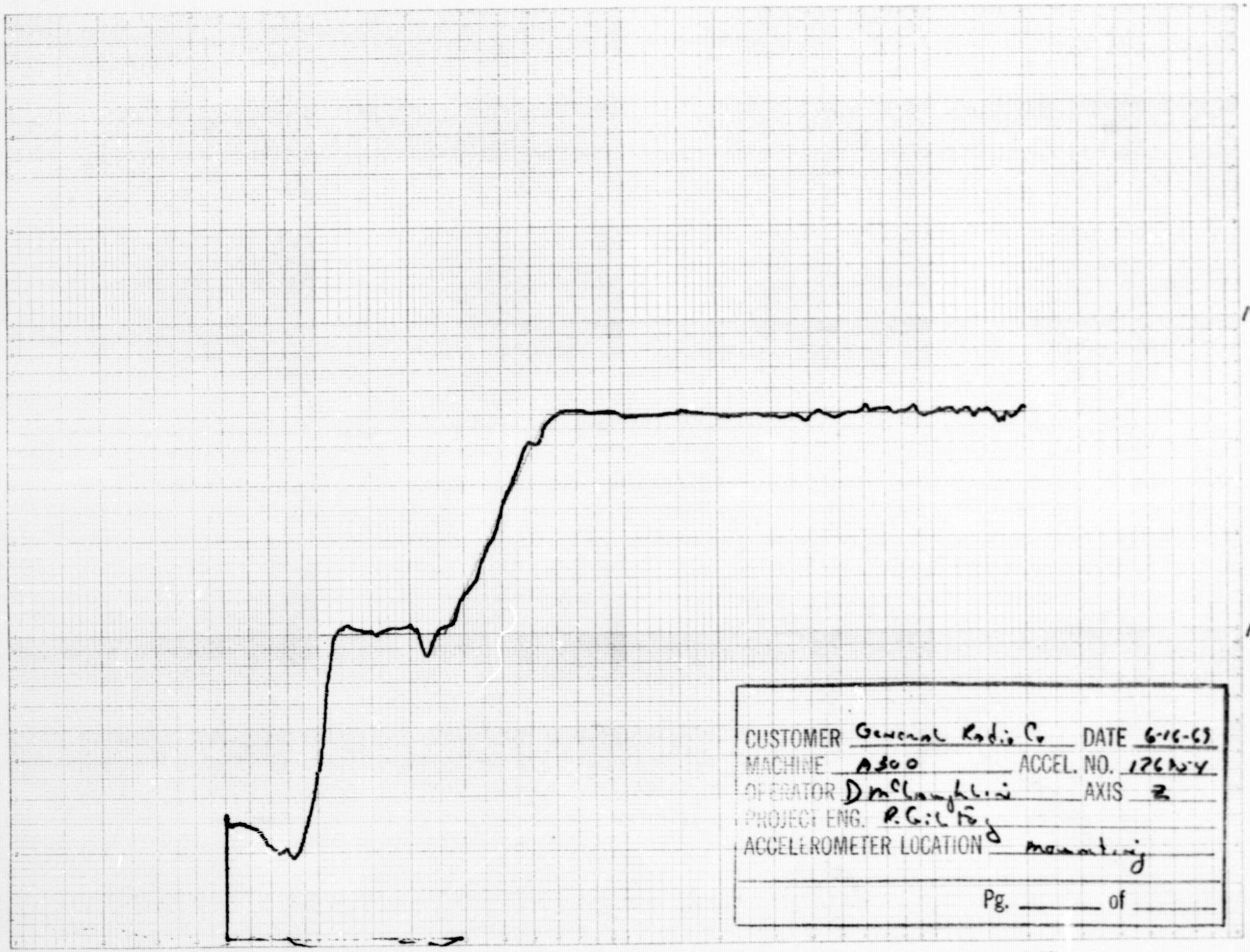
CUSTOMER General Radio DATE 6-16-69
MACHINE A300 ACCEL. NO. 1760-V
OPERATOR DMcLaughlin AXIS X
PROJECT ENG. RG. Lai & mounting
ACCELEROMETER LOCATION

Pg. _____ of _____



CUSTOMER General Radio Co. DATE 6-16-61
MACHINE A300 ACCEL. NO. 126F5-4
OPERATOR DMcLaughlin AXIS Y
PROJECT ENG. R.G. Fox
ACCELEROMETER LOCATION mounting J

Pg. _____ of _____



CUSTOMER General Radio Co. DATE 6-16-69
MACHINE A500 ACCEL. NO. 176 N-Y
OPERATOR D McLaughlin AXIS Z
PROJECT ENG. R.G. Kelly
ACCELEROMETER LOCATION mounting

Pg. ____ of ____

DATE 6-[illegible]-69
CUSTOMER General Radio Co.
TEST ITEM P/N _____ CODE _____
SERIAL NO. _____
CONDITION non operating
TEMPERATURE _____ PERIOD OF TEST _____ MIN.

OPERATOR D. McLaughlin
TEST ENGINEER R. C. Fuga
TYPE OF TEST _____
SPEC. NO. _____ PARA. _____
G RMS OVERALL 12.3
CHANNEL NO.

MACHINE NO. A300 S/N 27
CONTR. ACCEL. NO. 4335 S/N 17660-4
CONTR. ACCEL. LOCATION monitoring
AXIS EXCITATION X
PICK UP SENSING _____ AXIS
PICK UP SENSITIVITY _____ MV RMS
G'S PK

TEST NO. _____
ITEM _____ DATE _____
CODE _____ S/N _____

10 db

TEST NO. _____
PHASE _____
.1

SPECTRAL DENSITY
g^2/cps

CURVE NO. _____
.01

10 Hz

2000 Hz

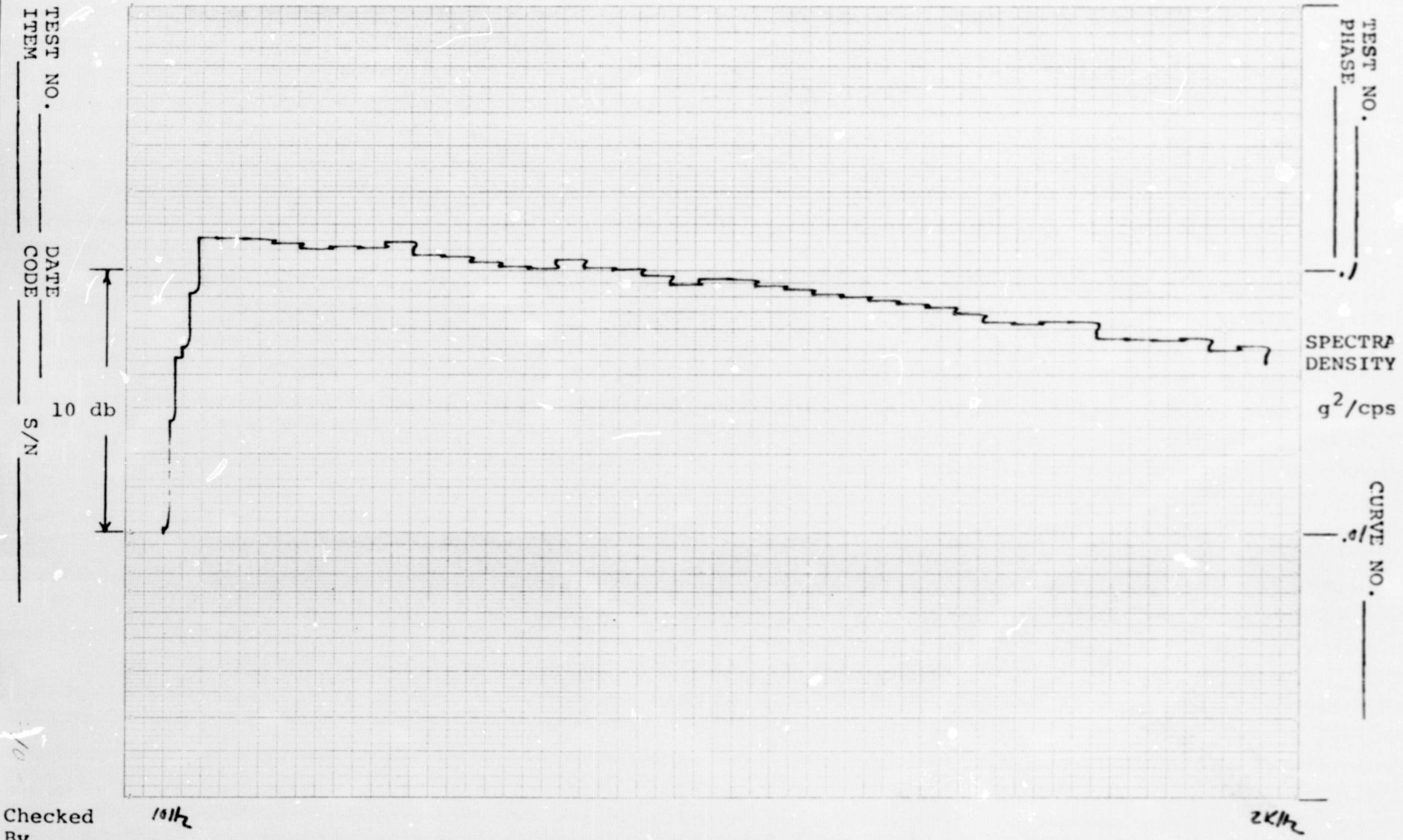
Checked By _____
Witness _____
Witness _____

HZ RANDOM VIBRATION

DATE 6- - 69
CUSTOMER General Radio Co.
TEST ITEM P/N _____ CODE _____
SERIAL NO. _____
CONDITION Non operating
TEMPERATURE _____ PERIOD OF TEST _____ MIN.

OPERATOR DMcLaughlin
TEST ENGINEER R.G.Kelly
TYPE OF TEST _____
SPEC.NO. _____ PARA. _____
G RMS OVERALL 12.3
CHANNEL NO.

MACHINE NO. A300 S/N 59
CONTR. ACCEL.NO. 4335 S/N 6F04
CONTR. ACCEL.LOCATION Armature
AXIS EXCITATION Y V
PICK UP SENSING _____ AXIS
PICK UP SENSITIVITY _____ MV RMS
G'S PK



Checked By _____
Witness _____
Witness _____

HZ RANDOM VIBRATION

DATE 6-4-69
CUSTOMER General Radio
TEST ITEM P/N _____ CODE ____
SERIAL NO. _____
CONDITION non operating
TEMPERATURE _____ PERIOD OF TEST ____ MIN.

OPERATOR D McCarty
TEST ENGINEER P.E. Kelly
TYPE OF TEST _____
SPEC.NO. _____ PARA. _____
G RMS OVERALL 12.3
CHANNEL NO.

CONTR. ACCEL.NO. 4335 S/N 176854
CONTR. ACCEL.LOCATION primary
AXIS EXCITATION Z
PICK UP SENSING _____ AXIS
PICK UP SENSITIVITY _____ MV RMS
G'S PK

TEST NO. _____
ITEM _____
DATE _____
CODE _____

10 db

SPECTRAL DENSITY
g^2/cps

TEST NO. _____
PHASE _____

CURVE NO. 1

10 HZ

2K HZ

Checked By _____
Witness _____
Witness _____

HZ RANDOM VIBRATION

DATE 6-[illegible]-69
CUSTOMER General Radio Co.
TEST ITEM P/N _____ CODE _____
SERIAL NO. _____
CONDITION Non operating
TEMPERATURE _____ PERIOD OF TEST _____ MIN.

OPERATOR D. McLaughlin
TEST ENGINEER R.G. Fay
TYPE OF TEST _____
SPEC.NO. _____ PARA. _____
G RMS OVERALL 5
CHANNEL NO.

CONTR. ACCEL.NO. 4335 S/N 1680-4
CONTR. ACCEL.LOCATION Mounting
AXIS EXCITATION X
PICK UP SENSING _____ AXIS
PICK UP SENSITIVITY _____ MV RMS
G'S PK

TEST NO. _____
ITEM _____
DATE _____
CODE _____

10 db

.01

SPECTRA DENSITY
g^2/cps

.001

CURVE NO. _____

10Hz

2000Hz

Checked By _____
Witness _____
Witness _____

HZ RANDOM VIBRATION

DATE 6-1 69
CUSTOMER Kearfott Radio Co.
TEST ITEM P/N _____ CODE _____
SERIAL NO. _____
CONDITION non operating
TEMPERATURE _____ PERIOD OF TEST ____ MIN.

OPERATOR P. McCrumb
TEST ENGINEER P. McCrumb
TYPE OF TEST _____
SPEC. NO. _____ PARA. _____
G RMS OVERALL 5
CHANNEL NO.

CONTR. ACCEL. NO. 4344 S/N 69
CONTR. ACCEL. NO. 4335 S/N 1.0 Fs=4
CONTR. ACCEL. LOCATION main trunnion
AXIS EXCITATION Y
PICK UP SENSING _____ AXIS
PICK UP SENSITIVITY _____ MV RMS
G'S PK

TEST NO. _____
ITEM _____
DATE _____
CODE _____
N/S _____

10 db

TEST NO. _____
PHASE _____
.01

SPECTRAL DENSITY
g^2/cps

CURVE NO. .001

Checked By _____
Witness _____
Witness _____

10 Hz

2K Hz

HZ RANDOM VIBRATION

DATE 6-[illegible]-69
CUSTOMER General Radio
TEST ITEM P/N _____ CODE _____
SERIAL NO. _____
CONDITION Non operating
TEMPERATURE _____ PERIOD OF TEST _____ MIN.

OPERATOR [illegible]
TEST ENGINEER [illegible]
TYPE OF TEST _____
SPEC.NO. _____ PARA. _____
G RMS OVERALL 5-
CHANNEL NO.

CONTR. ACCEL.NO. 4334 S/N 176
CONTR. ACCEL.LOCATION Mounting
AXIS EXCITATION Z
PICK UP SENSING _____ AXIS
PICK UP SENSITIVITY _____ MV RMS
G'S PK

TEST ITEM _____ TEST NO. _____
DATE _____
CODE _____
S/N _____

10 db

TEST NO. _____
PHASE _____
.01

SPECTRAL DENSITY
g^2/cps

CURVE NO. _____
.01

-11-

Checked By _____
Witness _____
Witness _____

50Hz

2KHz

HZ RANDOM VIBRATION